DATANET Overview

DPS7000/XTA
NOVASCALE 7000

Communications: General

REFERENCE
39 A4 15DM 03

DPS7000/XTA NOVASCALE 7000 DATANET Overview

Communications: General

July 1990

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Preface

Bull's network processor, the Bull Datanet, with its operating system DNS, is the keystone of an OSI/DSA communications network. In such a network the Datanet can play the role of front-end processor, data concentrator or communications switch.

The role it plays is determined partly by its hardware components and partly by the software which is configured at system generation time.

This manual describes the basic machine structure of the Bull Datanet and introduces the hardware components involved. It has been written for people involved in networking hardware, with little experience of the Bull Datanet, but who are familiar with the basic concepts of data communications.

The companion volume of the present document is the DNS Concepts manual (39 A4 20DN). It describes the software aspects of this machine.

While it is understood that the needs of hardware and software technicians are often distinct and apart, the reader of the present manual would gain a greater depth of knowledge of his own subject by reading the companion volume.

NOTE: This manual gives an overview of Bull's network processors in the Bull Datanet family. In no way does it constitute a hardware configurator. For configuration information contact your local Bull representative.

MANUAL DIRECTORY

Manual Title **Order Number**

Complementary reading:

Bull Datanet and CpNet - Site Preparation Manual.....39 A1 8027
Site Preparation for Questar Terminals.....80 A4 7884

Operator's information:

Bull Datanet and CpNet - Operator's Handbook.....39 A1 17DM
DNS V4 - In/On-Line Tests Operator's Guide.....39 A2 26DN
DNS V4 - NOI Operator's Guide.....39 A2 25DN

For information on software aspects of the Bull Datanet, refer to:

DNS V4- Concepts.....39 A4 20DN
DNS Terminal Management.....39 A2 24DN

for which the following are pre-requisite reading:

DSA - Concepts.....39 A4 9725
DSA - Pocket Guide.....15 A4 9729

Further reading:

DSA - Terminology.....39 A4 8688
DSA Open Systems Facilities - Concepts.....39 A4 9793
Bull CpNet - Overview.....39 A4 30DM

For supplementary information refer to the manuals referenced in the following documents:

DNS V4 - Documentation Directory.....39 A4 27DN
DSA Documentation Directory.....39 A4 9726

The manuals listed above may be ordered from the following address:

BULL, CEDOC-DILOG
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Table of Contents

Illustrations

Figures

Tables

1. Introduction

The Bull Datanet is a high performance computer designed specifically as a data network processor. It operates as an intermediary system which allows remote terminals and host computers to communicate and thus provides distributed systems with complete networking facilities

The Bull Datanet and its operating system (DNS) are based on Distributed Systems Architecture (DSA) which is Bull's standard for the design of distributed systems. DSA conforms to international data communications standards, and in particular to the ISO reference model for Open Systems Interconnection (OSI).

The DN 713X series of the Bull Datanet has been improved to satisfy users' needs in several areas, including:

- greater communications capacity,
- increased line speeds and machine throughput,
- improved maintainability,
- reduced cost,
- easy expandability.

In order to satisfy these requirements, the Bull Datanet is offered as a range of models based on a common, modular, hardware set.

1.1 ROLES OF THE BULL DATANET

Within a distributed environment, the Bull Datanet can operate as front end processor, data concentrator, communications switch or LAN gateway or any combination of these roles. The role of a Datanet in a given environment is determined by its hardware and software configurations.

It may be noted that for systems where the front end function is not required, Bull also offers the CpNet system model CN 5105 (refer to the Bull CpNet - Overview manual). This is a stand-alone communications processor which can operate as concentrator, switch or LAN gateway. The Bull CpNet is based on the same hardware packaging as the model DN 7130 Datanet.

1.1.1 Front End Processor

As a Front End Processor (FEP), the Bull Datanet provides networking services to one or several host computers to which it is attached. Host computers are connected via direct high speed channels to the Datanet (figure 1-1).

The Datanet provides the communications link between applications located in the host and other remote processors or terminals. Thus the resources of the host are freed for user applications.

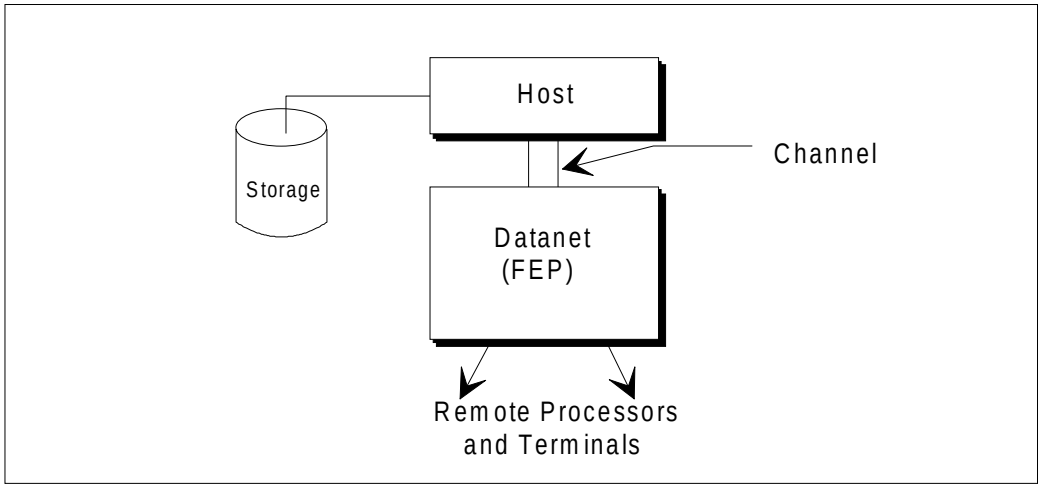


Figure 1-1. Bull Datanet Front End Processor (FEP)

1.1.2 Concentrator

A concentrator provides terminals (and possibly small computers emulating terminals) with access to distributed data processing resources (figure 1-2).

A large number of terminals and terminal types can be connected to a Bull Datanet through a variety of communication lines and networks. The group of terminals connected to a given processor is called the secondary network.

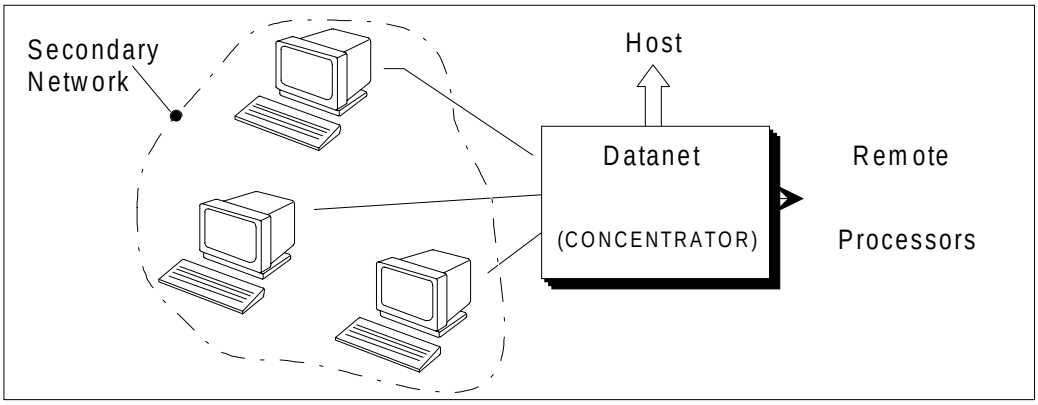


Figure 1-2. Bull Datanet Concentrator

1.1.3 X.25 Switch

X.25 switching is a routing mechanism which permits X.25 data packets to be routed between remote systems. Figure 1-3 shows several possibilities of NETWORK USERS (NU) which generate X.25 packets:

- a Bull Datanet front end processor,
- a Bull DPS 6
- the .i.PAD; of an X.25 public data network,
- an X.25 synchronous terminal cluster,
- an OSI/DSA workstation (DIWS, e.g. a Bull Questar 400),

Data from one system addressed to a second system can be routed via one or several switches, generally without the data having to be examined or processed by the switch system(s).

Several Bull Datanets operating as switches can be linked to form a private X.25 network. This facility is particularly useful for routing optimisation and back up.

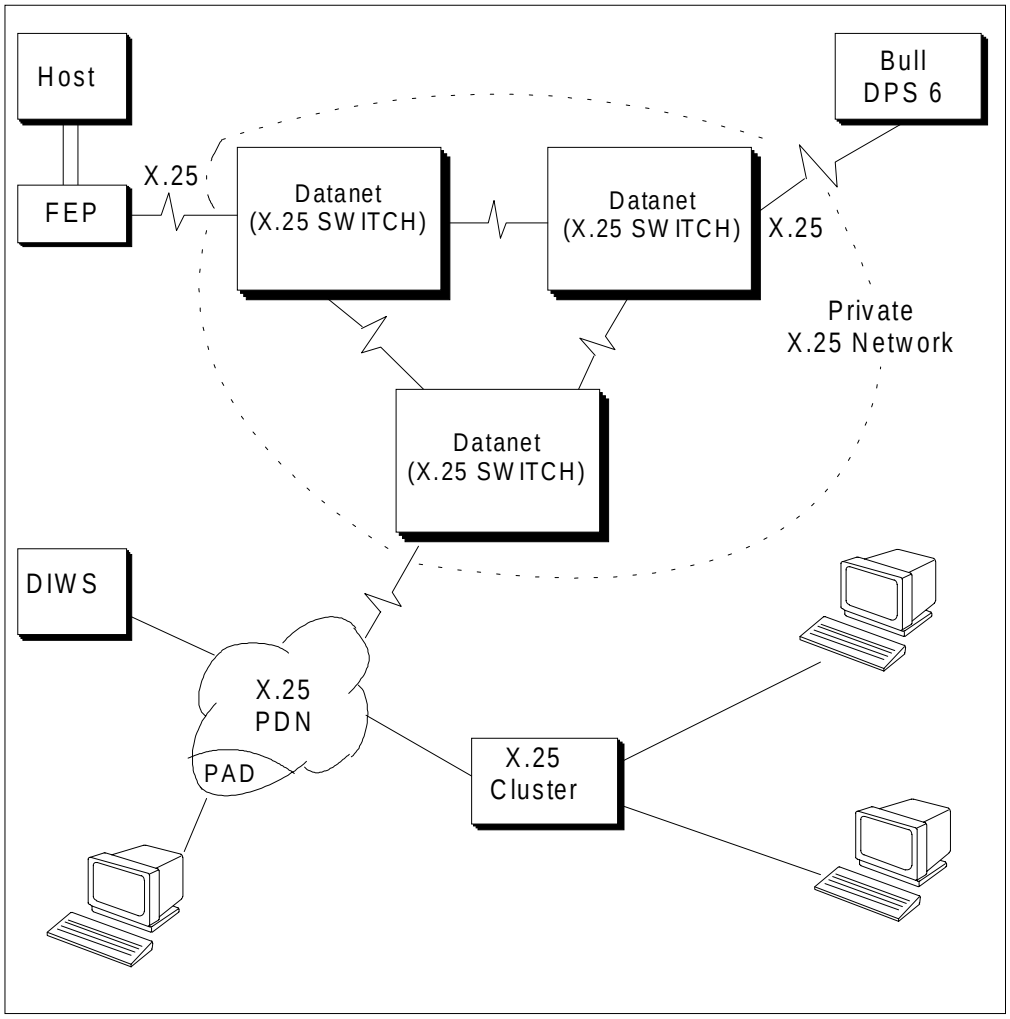


Figure 1-3. Bull Datanet X.25 Switch

1.1.4 Network Gateway

The Bull Datanet can communicate via both Wide Area Networks (WAN) and Local Area Networks (LAN). It can also provide gateway services between a WAN and a LAN. Two distinct configurations are possible.

Figure 1-4 shows a Datanet operating as the gateway between a systems on either a StarLAN or an E-LAN and an X.25 network user. In this case, the Datanet switches X.25 packets via the LAN. Note that, several different types of network user can generate X.25 packets (paragraph X.25 Switch).

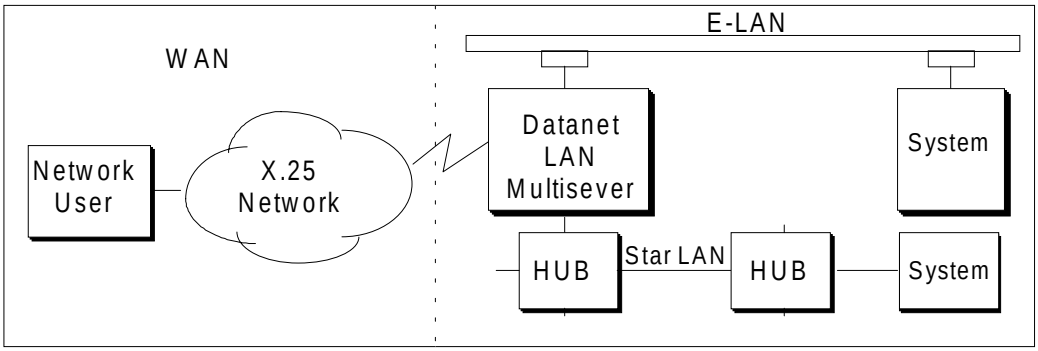


Figure 1-4. Bull Datanet Network Gateway

Figure 1-5 shows a Datanet operating as the gateway between a remote host on a point to point HDLC line and either a StarLAN or an E-LAN System. The Datanet plays the role of communications router and media adapter.

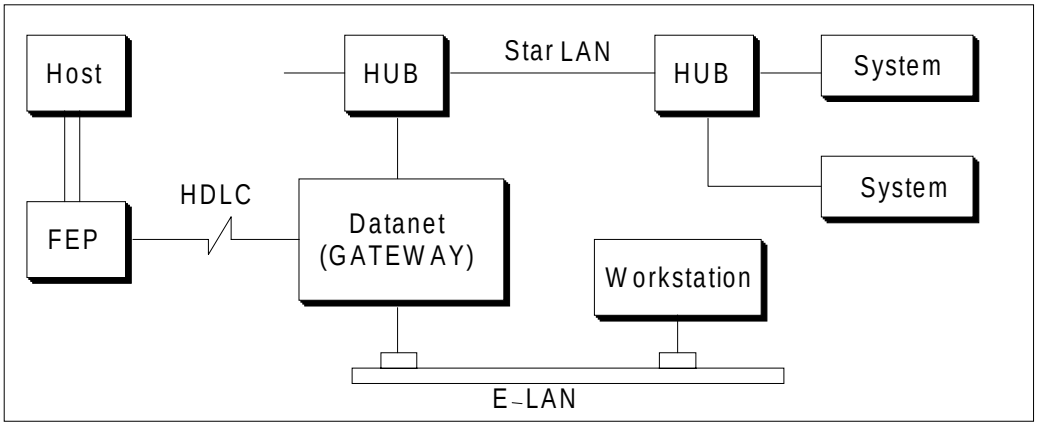


Figure 1-5. Bull Datanet Network Gateway (2)

Note that the two configurations described above are fundamentally different. In the first case, the gateway is switching X.25 packets via the LAN (PACKET SWITCHING). In the second case, X.25 techniques are not used, the gateway system is routing messages (MESSAGE SWITCHING). Further details of these two concepts are given in the DNS - Concepts manual.

Certain models of Bull Datanet support two LAN connections. Thus the Datanet can also operate as a gateway between two LANs, as shown in figure 1-5.

1.1.5 Administrative Tool

The Bull Datanet provides administration services. These are application programs used for network control, testing, monitoring and statistics gathering. The programs are located within the processor itself. Their distribution in every node of a network provides a coherent vision of the network to the people responsible for supervising its operation.

1.2 COMPONENTS OF THE BULL DATANET SOFTWARE

The Distributed Network Supervisor (DNS) is the operating system for the Bull Datanet. It is a configurable software package designed to manage network functions. It comprises a common nucleus and four main areas of activity:

- host systems management,
- primary network control,
- secondary network control,
- administration and other maintenance applications.

In a given system, these areas of activity may or may not all be used.

The DNS "logo" (shown in figure 1-6) is the traditional representation of this software. It shows the central nucleus surrounded by the 4 main activities.

While the discussions which follow are mainly concerned with the Bull Datanet hardware, frequent reference will be made to these convenient sub-divisions of the operating system.

The latest release of the DNS operating system is particularly important for its open system facilities. An OSI/DSA plug in the Datanet can provide access to DSA applications for systems in an OSI network, via the Datanet primary network control.

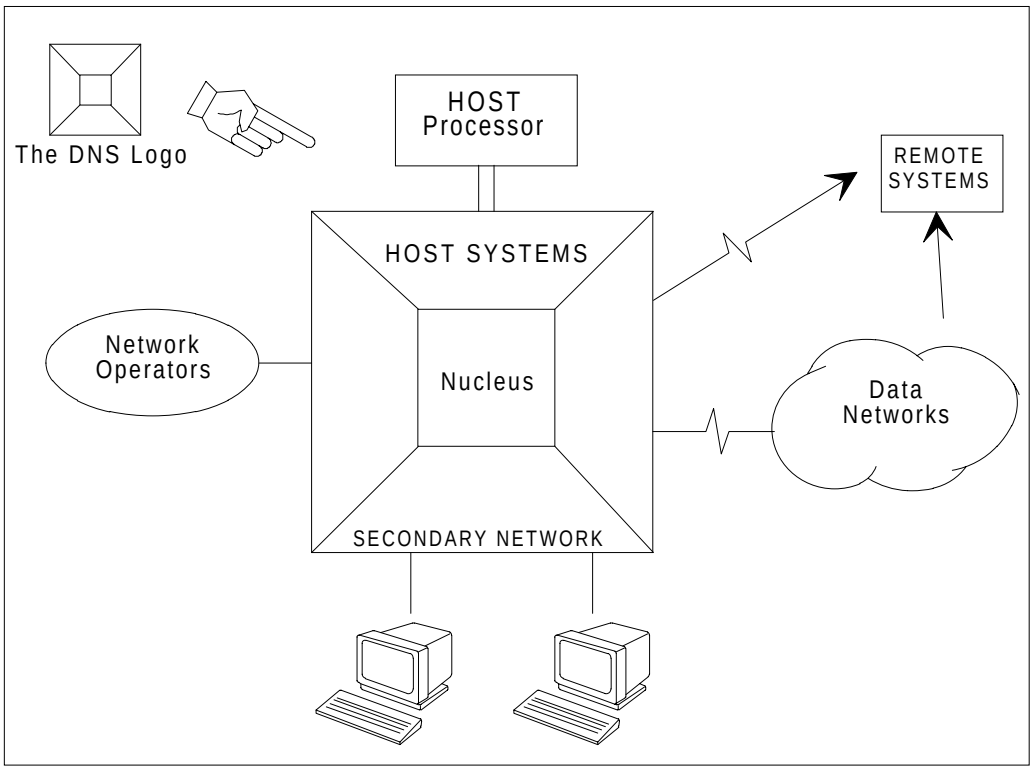


Figure 1-6. The Distributed Network Supervisor

Gateway software in the Datanet can provide conversion between DSA and SNA[TM] protocols, allowing remote IBM[TM] hosts to communicate with DSA systems in the Datanet primary network or with terminals in its secondary network.

Additionally, an IBM host may use the Datanet as a front-end processor, providing direct access to the DSA primary and secondary networks.

[TM] These abbreviations are trademarks of the International Business Machines Corporation.

1.3 TECHNOLOGIES SUPPORTED

1.3.1 Host Processor Support

The Bull Datanet can be used as a front-end processor for a variety of hosts. It supports not only Bull's own processors but also IBM SNA systems. Bull host systems that operate in a DSA network are:

- Bull DPS 8 family of systems (DPS 8, 88, 8000, 90 and 9000) running under the GCOS 8,
- Bull DPS 7/7000 systems running under GCOS 7.

It is possible to connect several Datanets to a single host or to connect one Datanet to several hosts. Also, it is possible to connect two different types of host to the same Datanet. The number of connections depends on the models of the host and Datanet.

For information on interconnections between the Datanet and other manufacturers' equipment, refer to the Open Systems Facilities - Concepts manual.

1.3.2 Primary Network Support

The term "Primary Network" refers to the connections between Bull Datanets, Bull DPS 6 distributed systems and Bull CpNets (see figure 1-7). Primary Network support covers both Wide Area Networks (WAN) and Local Area Networks (LAN). These networks are implemented using the architectural rules of the OSI reference model and are referred to as "OSI/DSA networks". Other manufacturers' systems conforming to the OSI standards can also be connected to an OSI/DSA network via the Datanet WAN support. For further information, refer to the DSA Concepts manual.

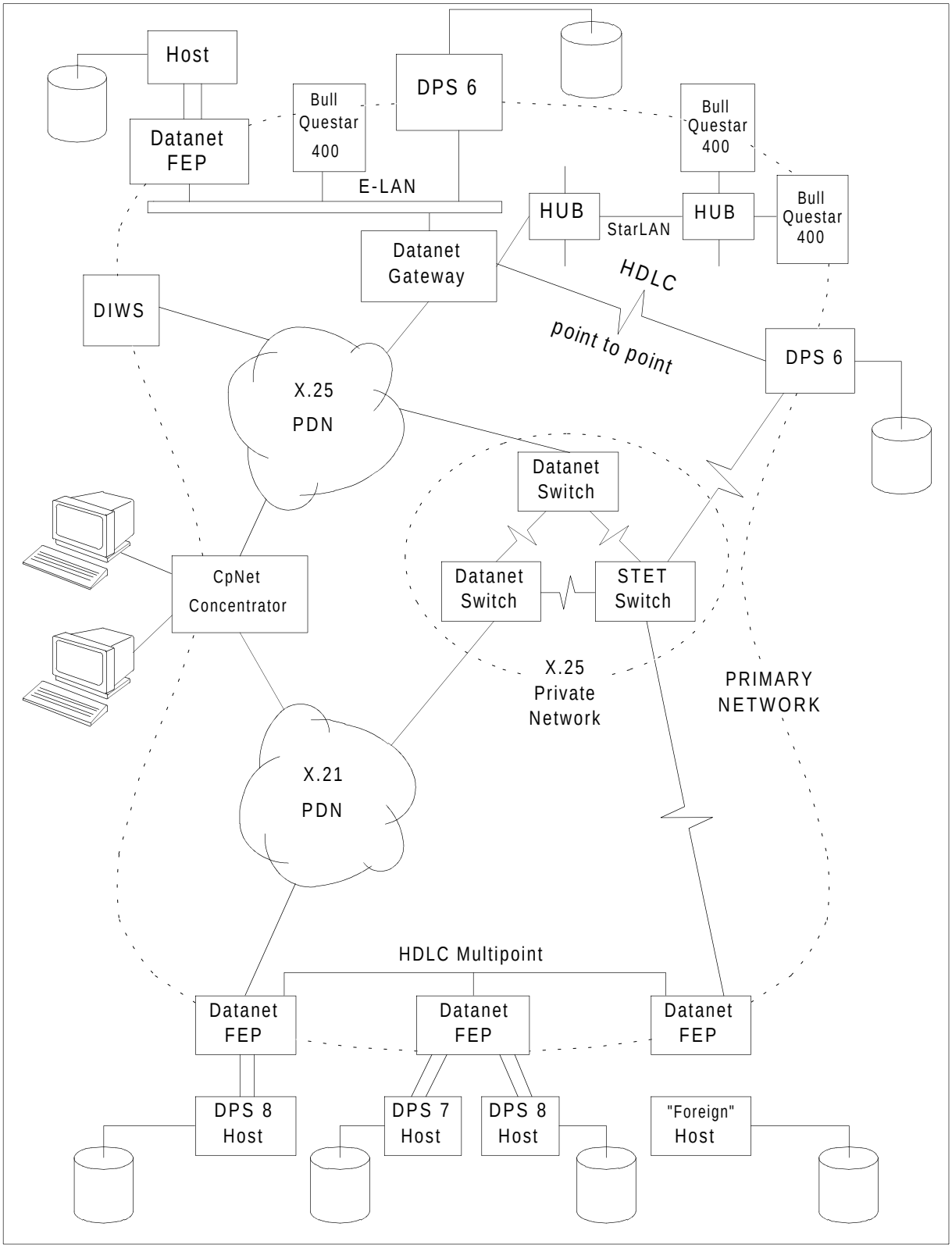


Figure 1-7. Primary Network

The Bull Datanet supports ISO 8802.2 and 8802.3 Local Area Networks as a solution to high speed communications between systems located in a single building or a building complex. These networks can be implemented either with StarLAN or E-LAN configuration.

1.3.2.1 Transmission techniques

The Bull Datanet supports the following types of communication links on WANs:

- point-to-point links using HDLC (LAP.B) protocol over dedicated (private or leased) or switched lines,
- multi-point connections using HDLC (NRM, also called LAP.N) protocol on links between Bull Datanets and CpNets.
- packet switching over PDN/VAN or private (OSI/DSA) networks using the StarLANX.25 protocol,
- circuit switching on X.21 public data networks.

In addition, certain Datanet models support Bull's new Single Line Communications Controller (SLCC) which has been developed for communications over high speed lines using X.21 or V.35 interfaces at a maximum speed of 2 Mbit/s. The SLCC provides earth links between Datanets and CpNets. It also provides access to telecommunications satellite links such as the French Telecom 1 for file transfer and remote batch facilities.

Local Area Networks supported by the Bull Datanet comply to the ISO 8802.2 and 8802.3 recommendations and operate at speeds from 1 Mbit/s to 10 Mbit/s.

1.3.2.2 Types of Network

The Bull Datanet supports public data networks for which OSI/DSA provides an external interface which include those shown in table 1-1.

Table 1-1. PDNs presently supported by the Bull Datanet (1/2)

X.25 Packet Switching Networks	
Name	**Country**
ARPAC*	Argentina
AUSTPAC	Australia
DATEX-P*	Austria, West Germany
DCS*	Belgium
CNCP	Canada
DATAPAC	Canada
DATAPAK*	Scandinavian countries
TRANSPAC*	France
ITAPAC	Italy
DDX-P	Japan
VENUS-P	Japan
LUXPAC*	Luxemburg

Table 1-2. PDNs presently supported by the Bull Datanet (2/2)

X.25 Packet Switching Networks	
Name	**Country**
SCT	Mexico
DN 1*	Netherlands
TELEPAC*	Portugal
IBERPAC*	Spain
TELEPAC*	Switzerland
PSS	United Kingdom
TELENET	USA
TYMNET	USA
UNINET	USA
INFONET*	World-wide
X.21 Circuit Switching Networks	
Name	**Country**
DATEX-L	Austria, West Germany
DDX-C	Japan
DATEX*	Scandinavian countries
TRANSCOM*	France
TRANSDYN*	France

* Bull Datanet support of these networks has been qualified by Bull. The other public data networks mentioned

above conform to the interface of the Bull Datanet.

1.3.3 Secondary Network Support

The "secondary network" of a Bull Datanet is the name given to all the terminals and their associated connections under the control of this system. Secondary network support manages the physical support of the terminals, the link procedure and conversion to OSI/DSA protocols.

The Datanet provides terminals with an access point into an OSI/DSA (primary) network. Gateway facilities also provide access to IBM SNA systems. Terminals can access applications located in local or remote hosts and can communicate with other terminals in the network.

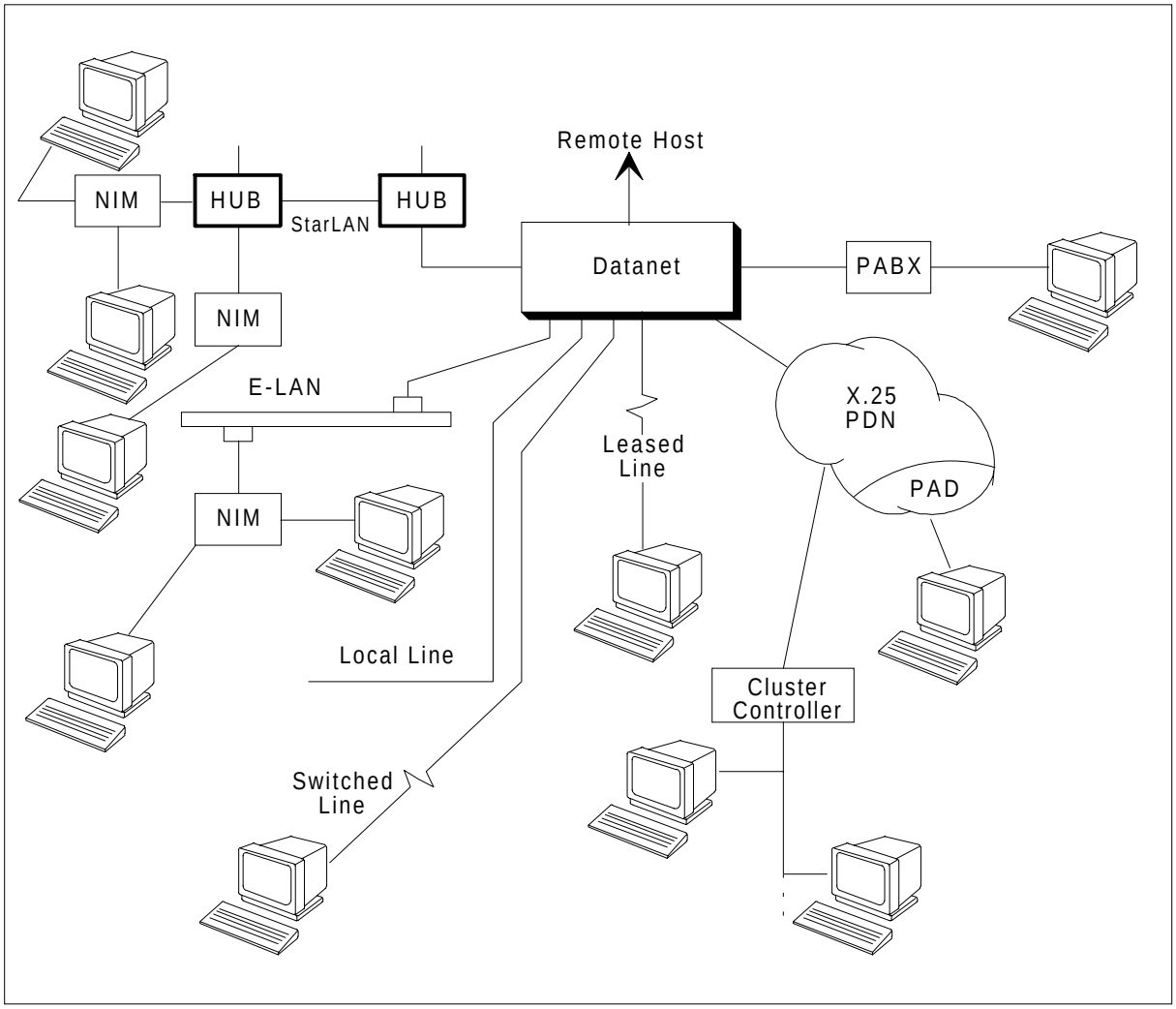


Figure 1-8. Secondary Network

These terminals can be connected directly to the Datanet or via telecommunications facilities (dedicated, switched or public network lines) including digital Private Automatic Branch Exchanges (PABX), and both StarLAN and E-LAN Local Area Networks using the Network Interface Module (NIM) for asynchronous terminals, as shown in figure 1-8.

Also, for synchronous terminals, a group of devices (called a "cluster") can be connected to a single line or network via a cluster controller. This facility is particularly useful for network optimisation since it permits the use of a single line for several devices, instead of one line to each device.

Terminals supported by the Datanet are shown in table 1-2 at the end of section 1. Existing line protocols such as the VIP screen presentation protocol, the TTY procedure used by printers and remote batch procedures for computers in the secondary network (BSC 2780/3270/3780, etc.) are supported.

New communications techniques such as the X.29 protocol used by asynchronous PAD and Videotex terminals (e.g. Minitel in France) are also handled. Terminals operating under these protocols thus become correspondents in a OSI/DSA network.

1.4 COMPONENTS OF THE BULL DATANET HARDWARE

The Bull Datanet hardware is divided into three subsystems, as shown in figure 1-9:

- Central Subsystem.
- Host Subsystem.
- Communications Subsystem.

Each subsystem comprises a number of modules which support the various functions of the Datanet. Communications of data and instructions between these modules take place via the high speed Megabus.

A brief introduction to each of the subsystems is given below. For further details concerning the individual modules refer to section 3.

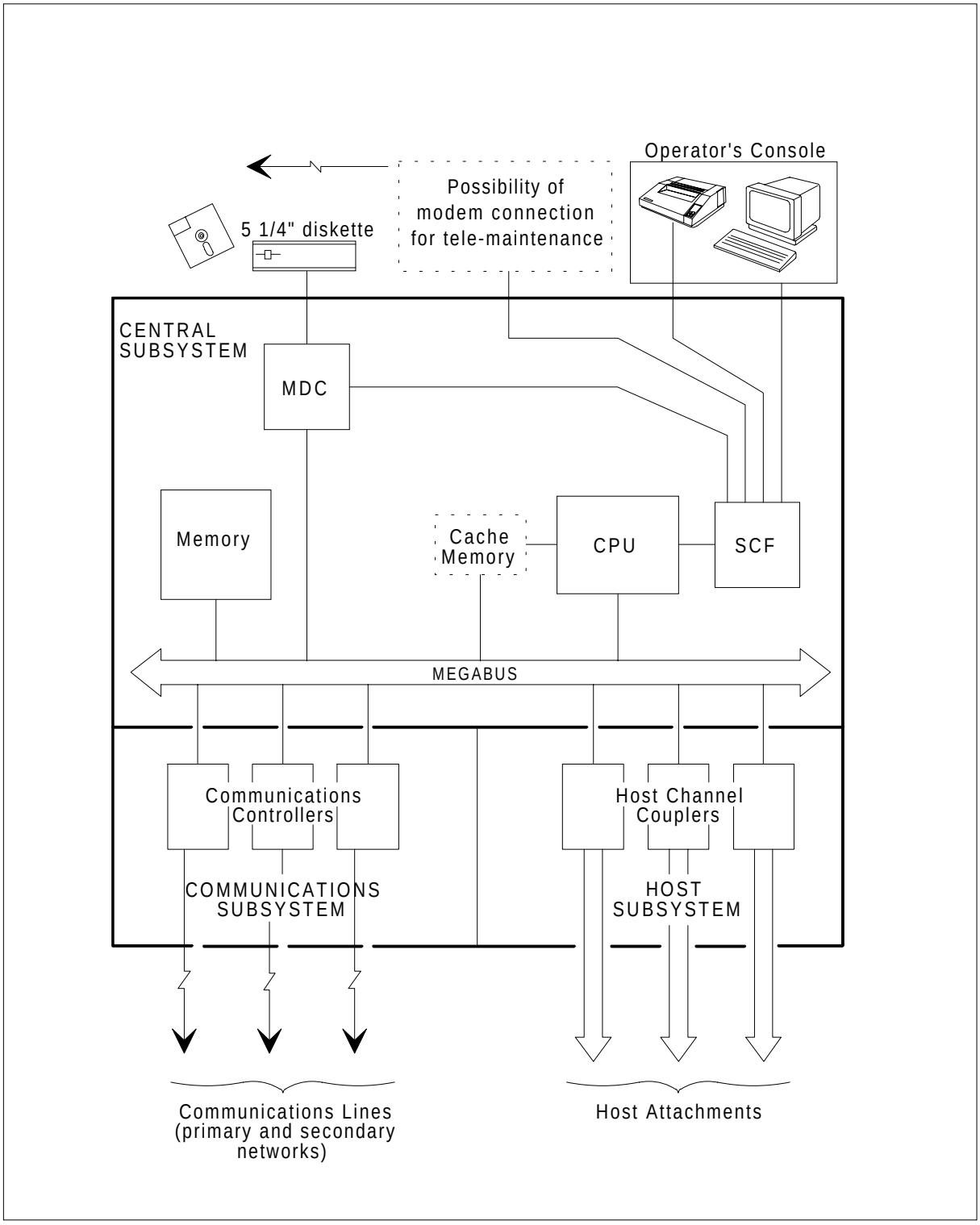


Figure 1-9. The Bull Datanet Hardware Subsystems

1.4.1 Central Subsystem

The central subsystem provides the Bull Datanet processing power. The standard system memory contains the DNS software, provides data buffering and may contain applications such as in/on-line tests. Memory size may be increased by the addition of an optional module and, on certain systems, memory access time may be reduced by the addition of a cache memory system. Information exchange between memory and the other subsystems is performed using Direct Memory Access (DMA).

The CPU executes the instructions and responds to operator's commands entered at the console and transferred via the SCF (see below). Processing power may be increased on certain systems by the addition of a second CPU (the Attached Processor).

The System Control Facility (SCF) is the operator's interface with the system. It dialogues with the software running in the Datanet and exchanges messages and commands with the operator's console. The SCF is generally connected to a local operator's console comprising a screen, keyboard and hardcopy printer. Connection of a remote console via a modem is also possible, to provide tele-maintenance facilities.

The standard diskette drive (5,25 inch, 640 kbyte) operates under control of the Multi-Device Controller (MDC). It may be used for loading and dumping the operating system, loading test programs or as a back-up network log-file. An optional second diskette may be fitted if required.

1.4.2 Host Subsystem

The host subsystem provides the hardware elements of the Bull Datanet host systems management. Three types of channel coupler provide communications with both Bull and IBM SNA host systems.

1.4.3 Communications Subsystem

This subsystem comprises controllers for the various communications lines connected to the Bull Datanet. It comprises both the secondary and primary (wide area and local area) network control.

Table 1-3. Terminals Supported by the Bull Datanet

Synchronous Terminals and Controllers	Associated Displays	Associated Printers
ASPI10V, 30V, 34V, 38V		
Bull QUESTAR 210		PRU 708x
Bull QUESTAR 400	- using MSTE 7107/VIP	
Bull Micral xx	-in DKU 7105/7107 emulation mode (Micralink 7105) - in DKU 7005 emulation mode	
TTX 35		
TCS 74X4	DKU 7107 DKU 7211 TWS 2107 TWS 2207 TWS 2307	PRT 7203 PRT 722X PRT 723X PRT 7239
DKU 7005		TTU 812X
DKU 7105		PRU 7080
DKU 7205		PRT 722X
TCU 7021		TTU 812X
TCU 7032	DKU 7007	PRU 708X
TCU 7042/44	DKU 7107	PRT 722X
TCU 7046/47	DKU 7211	PRT 7121 (for TCU 7032 only)
TCU 7052/54		
TTU 8221,8223		
TTU 8229		
TWS 2105, 2205		PRT 7203 PRT 722X PRT 723X PRT 7239
VIP0000, 0001		
VIP7700, 7760		
VIP7804, 7805		
VIP7814		

Table 1-4. Terminals Supported by the Bull Datanet (contd.)

Asynchronous Terminals
ASPI10, 32, 38
Bull QUESTAR 210
Bull Micral XX - in VIP 7800 emulation mode (MIMIC) Bull Micral XX - in 7102 presentation (Micralink 7102) HDS5, HDS5T, VIP 7814 DKU 7001
DKU 7002) in DKU 7001 emulation mode DKU 7102) DKU 7202)
TTU 8125/27 (also TTU 8124/26)
TTX 80/90
PRT 7220/7221
TWS 2102, 2202, 2302(color)
VIP7801, 7802, 7813
OTHERS : N.B. For a fully comprehensive list of terminals (see DNS Terminal Management Manual).
Synchronous BSC 3271 models 1 & 2 BSC 3274 model 1C, 21C, 31C, 41C, 51C, 61C BSC 3275 models 1, 2, 11 and 12 BSC 3276 models 1, 2, 3, 4, 11, 12, 13 and 14
Associated displays 3277, 3278, 3279, 3178, 3179, 3180
Associated Printers 3284, 3286, 3287, 3288, 3289 BSC 2780 BSC 3780
Asynchronous
MINITEL model TELIC 1

Table 1-5. Terminals Supported by the Bull Datanet (contd.)

X.25 Terminal Controllers	Associated Displays	Associated Printers
Bull QUESTAR 400	- using MSTE 7107/X.25	
TCS 74X6	TWS 2107 TWS 2207 TWS 2307	PRT 720X PRT 722X PRT 723X PRT 7239
TCU 7022	DKU 7007	TTU 812X
TCU 7043/45	DKU 7107	PRU 708X
TCU 7053/55	DKU 7211	PRT 722X

2. Hardware Configurations

The DN 71XX series of Bull Datanet provides a complete spectrum of processing power and communications capabilities. Each system is adapted to specific needs in terms of processing power and data communications capabilities.

The standard model at the bottom of the range is the DN 7130 which is of particular interest to the users of small networks. It is provided with minimum data communications facilities and has been designed primarily as a FEP for entry level Bull DPS mainframes.

Systems at the top end of the range are designed with increased central processing power and extensive communications facilities. These processors are the ideal communications components for large networks linking the most powerful Bull host processors.

2.1 THE BULL DATANET RANGE

The Bull DN 71XX series of processors constitutes an extensive range of processing power and communication facilities. Each model is delivered as a preconfigured package. For full details of dimensions, weight and electrical power consumption, refer to the Bull Datanet and Bull CpNet Site Preparation Manual. Figure 2-1 shows the physical appearance of these systems:

- the Bull DN 7130 is housed in 30 inch high lowboy cabinets.
- the Bull DN 7131 and DN 7100/20 are housed in one 60 inch high standard cabinet.
- the Bull DN 7100/40 is mounted in two 60 inch high cabinets having a total width of 51 inches. The Bull DN 7100/40 may optionally be fitted with a third cabinet, necessary if its full communications capacity is used.

The hardware modules of the host subsystem and communications subsystem are common to the whole range of Bull Datanets. The major difference between models lies in the type of central subsystem (CSS) used. The low range models are based on an integrated central subsystem, the CR41 CSS which is a single board comprising CPU, main memory and system control facility (SCF). The top of the range models contain discrete boards for each of these units. In addition, these models are equipped with a second CPU and cache memory.

The standard and optional modules contained in each Bull Datanet model are listed in the following paragraphs. Further details on each module will be found in section 3. All models are configured with at least one host channel attachment. This channel provides a useful facility for load, dump and network administration functions.

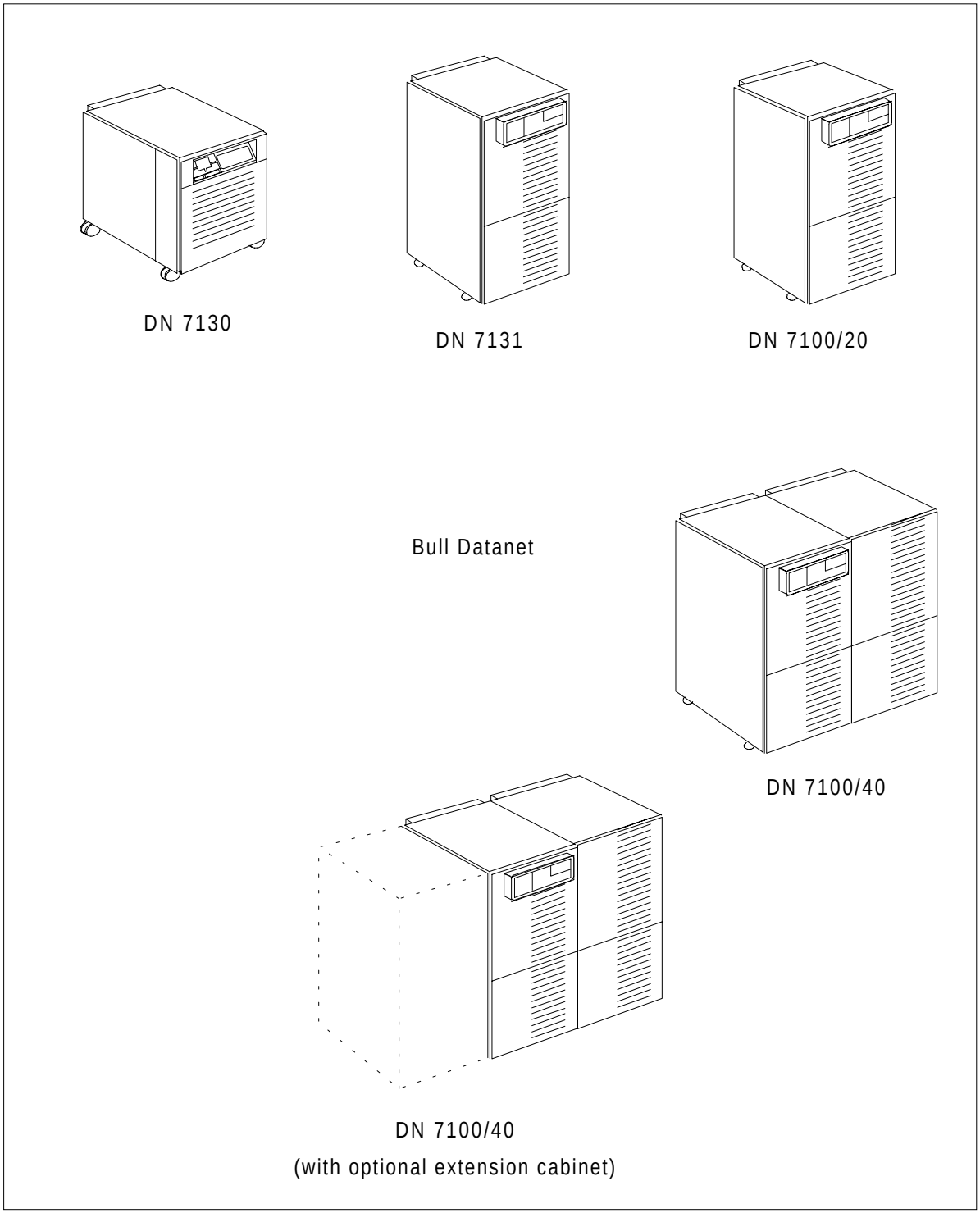


Figure 2-1. The Bull Datanet Range

2.1.1 Host Channels Supported

Depending on the model number, the Bull Datanet may support up to four host channel connections. Channels supported include the following:

- DIA channel (Direct Interface Attachment) to the Bull DPS 8 family of hosts,
- PSI channel (Peripheral System Interface) to Bull DPS 7 hosts,
- CIU channel (Channel Interface Unit) to IBM S370 (except models 115/125), 303X, 4331, 4341, 308X or 3090 hosts.

In addition, where multiple host connections are permitted, the Bull Datanet may be connected to several different types of host (a maximum of two different types) or may be connected to a single host via more than one channel (useful for back-up).

2.1.2 Communications Lines Supported

When considering the maximum configuration of a Bull Datanet, the following points should be borne in mind:

- one MLX-16 communications controller can support 4 line adapters (LA), maximum.
- one LA can support a maximum of:
  - either 4 synchronous or 4 asynchronous lines,
  - or 2 HDLC lines via a V.24 interface,
  - or 1 HDLC line via a V.11, V.35 or X.21 interface.
- one MLX-16 controller is fitted as standard to the 7100/20 and 7100/40 Bull Datanet models,
- two MLX-16 controllers are fitted as standard to the 7130 Bull Datanet model,
- three MLX-16 controllers are fitted as standard to the 7131 Bull Datanet model,
- one LA is fitted as standard to the first MLX-16 and it is used exclusively for the BPF and 3 synchronous V.24 lines,
- the Boot PROM FLAP (BPF) is fitted as standard to the first line position of this LA. The 3 synchronous lines are for customer use. Thus all Bull Datanets can be connected to at least 3 synchronous lines,
- one SLCC communications controller supports 1 (high speed) line, only the top of the range models support this controller,
- one Dual LAN controller supports two Local Area Networks, either one E-LAN and one StarLAN, or two StarLANs.

On certain models, due to physical restrictions, the Dual LAN controller is fitted in place of an MLX-16, an SLCC or a host channel coupler. The maximum number of controllers and lines depends on the Bull Datanet model, as described in the following paragraphs.

2.1.3 Tele-Load/Dump

Apart from load and dump from the system diskette or from a local host, the Bull Datanet can be loaded or dumped from a remote system.

This remote system may be a host or a network control centre. In either case the Datanet must be loaded via a "loader" system which is either another Datanet or a Bull CpNet. The "loader" system may be connected to the "loaded" system via:

- an HDLC point to point communications line,
- or over an Ethernet type Local Area Network, only.

The load/dump process is executed under control of a firmware routine implemented on the Boot Prom FLAP (BPF).

The Teleload/dump process is standard on DN7100/20 and DN7100/40 and optional on DN7130 and DN7131.

2.2 MODEL DN 7130

The DN 7130 is the first model in the Bull Datanet range. It has been designed for host systems requiring minimum communications facilities. Of particular interest is the improved price/performance ratio. The functional layout of this system is shown in figure 2-2.

2.2.1 The Basic Machine

The following components are fitted as standard to the DN 7130:

- Central subsystem
  - CR41 CSS provided with 1 Mbyte of memory and SCF PROMs,
  - Boot PROM FLAP (BPF) for host and diskette loading,
  - Multi-device controller (MDC),
  - one 5,25 inch diskette drive (650 kbyte),
  - operator's console,
- Communications subsystem
  - two MLX-16 communications controllers,
  - one LA fitted to the MLX-16. The first line of this LA is fitted with the BPF,

The following components are mandatory add-ons to the DN 7130:

- one host channel coupler (DIA, PSI or CIU) if used as a FEP.

2.2.2 Options

The following equipment may be added to the basic DN 7130:

- Central subsystem
  - 1 Mbyte memory extension,
  - Extended BPF for host, diskette and tele-loading,
  - a second 5,25 inch diskette drive (650 kbyte),
- Communications subsystem
  - three LA (for sync, async. or HDLC lines) for the first MLX-16 controller,
  - four LA (for sync, async. or HDLC lines) for the second MLX-16 controller,
- Host subsystem
  - none.

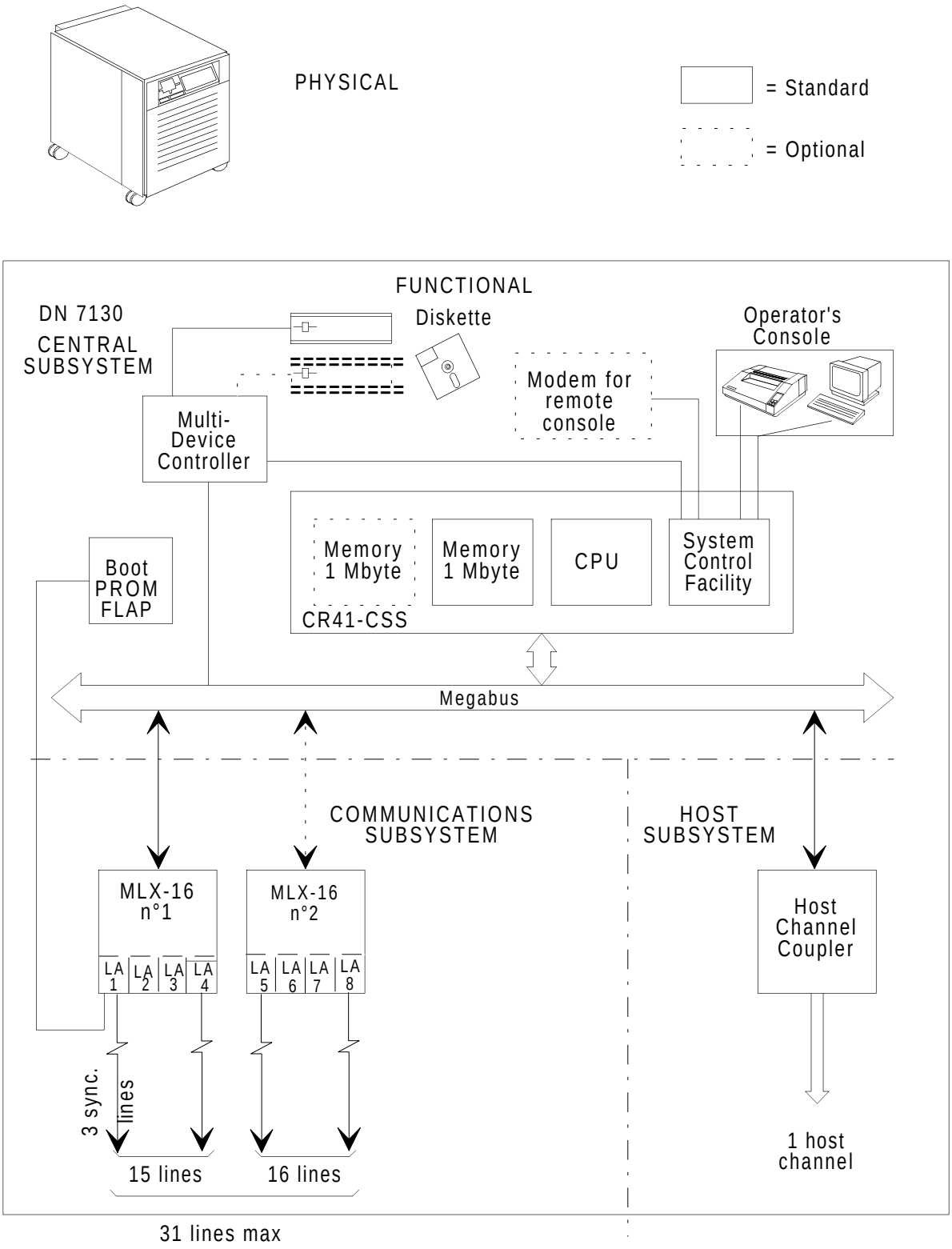


Figure 2-2. DN 7130 Configuration

2.2.3 Maximum Configuration

- Host subsystem

The host systems management of the DN 7130 supports one host channel connection.

- Communications subsystem

The DN 7130 can be fitted with a theoretical maximum of 7 optional line adapters for the MLX-16 controllers. This provides the following maximum configurations:

Sync. or Async. lines	HDLC lines (V.11, V.35, X.21)	HDLC lines (V.24)
31	0	0
3	7	0
3	0	14

All intermediate combinations are also possible.

As explained in section 3, the theoretical maximum may be reduced by the load factor of the lines used on the MLX-16 controllers.

2.3 MODEL DN 7131

This is the second model of the Bull Datanet range. It is based on the same central subsystem as the DN 7130 and therefore has the same processing power. Due to the larger cabinet, however, communications and host channel connections have been increased. Figure 2-3 shows the functional layout of the system.

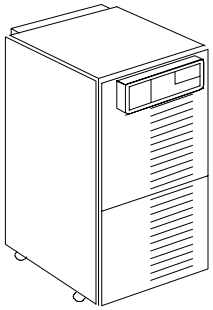
2.3.1 The Basic Machine

The following components are fitted as standard to the DN 7131:

- Central subsystem
  - CR41 CSS provided with 1 Mbyte of memory and SCF PROMs,
  - Boot PROM FLAP (BPF) for host and diskette loading,
  - Multi-device controller (MDC),
  - one 5,25 inch diskette drive (650 kbyte),
  - operator's console,
- Communications subsystem
  - three MLX-16 communications controllers,
  - one LA fitted to the first MLX-16. The first line of this LA is fitted with the BPF,

The following components are mandatory add-ons to the DN 7131:

- one host channel coupler (DIA, PSI or CIU) if used as a FEP.



PHYSICAL

= Standard

= Optional

FUNCTIONAL

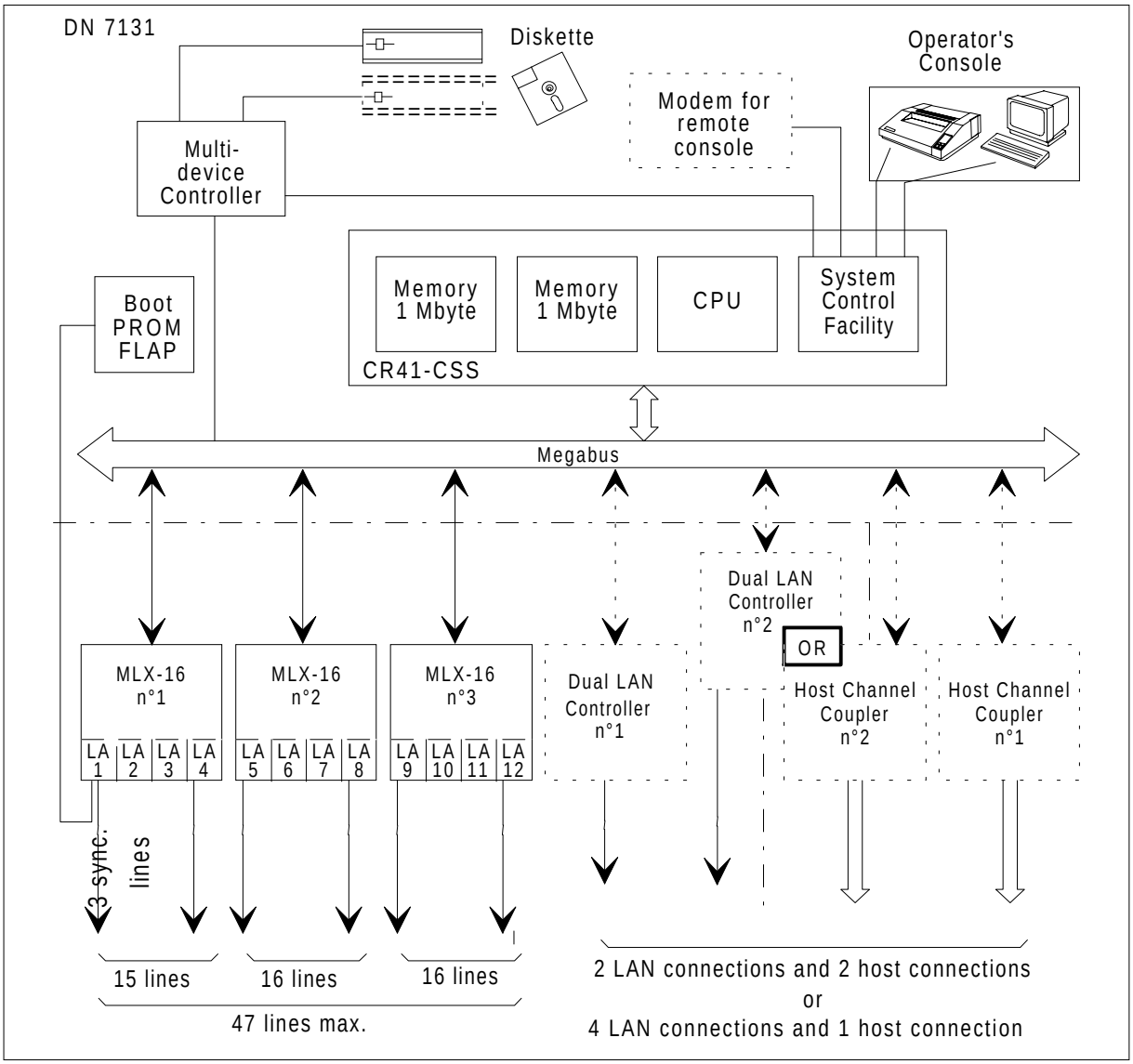


Figure 2-3. DN 7131 Configuration

2.3.2 Options

The following equipment may be added to the basic DN 7131:

- Central subsystem
  - 1 Mbyte memory extension,
  - extended BPF for host, diskette and tele-loading,
  - a second 5,25 inch diskette drive (650 kbyte),
- Communications subsystem
  - three LA (for sync, async. or HDLC lines) for the first MLX-16 controller,
  - four LA (for sync, async. or HDLC lines) for each additional MLX-16,
  - Dual LAN controller n° 1,
  - Dual LAN controller n° 2 in place of the second host channel coupler,
- Host subsystem
  - a second host channel coupler (in place of LAN controller n° 2).

2.3.3 Maximum Configuration

- Host subsystem

The host systems management of the DN 7131 supports a maximum of two host channel connections or only one host channel if two Dual LAN controllers are fitted.

- Communications subsystem

The DN 7131 can be fitted with a theoretical maximum of 11 optional line adapters for the MLX-16 controllers. This provides the following maximum configurations:

Synchronous or Asynchronous lines	**HDLC lines (V.11, V.35, X.21)**	**HDLC lines (V.24)**
47	0	0
3	11	0
3	0	22

All intermediate combinations are also possible.

As explained in section 3, the theoretical maximum may be reduced by the load factor of the lines used on the MLX-16 controllers.

In addition, the DN 7131 supports a maximum of 4 LAN connections (if only one host coupler is fitted).

2.4 MODEL DN 7100/20

This is the third model of the Bull Datanet range. It differs from the DN 7130 and DN 7131 in the technology used for the central subsystem. It has increased processing power and greater communications facilities compared with the DN 7131 and, in addition, it supports the new SLCC controller for high speed lines up to 2 Mbit/s. Figure 2-4 shows the functional layout of the system.

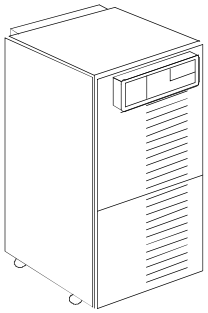
2.4.1 The Basic Machine

The following components are fitted as standard to the DN 7100/20:

- Central subsystem
  - two 7XE CPU,
  - 2 Mbytes of memory,
  - system control adapter board (SCA),
  - Boot PROM FLAP (BPF) for host REMOTE and diskette loading,
  - Multi-device controller (MDC),
  - one 5,25 inch diskette drive (650 kbyte),
- Communications subsystem
  - one MLX-16 communications controller,
  - one LA fitted to the first MLX-16. The first line of this LA is fitted with the BPF,

The following components are mandatory add-ons to the DN 7100/20:

- operator's console,
- one host channel coupler (DIA, PSI or CIU) if used as a FEP.



PHYSICAL

= Standard

= Optional

FUNCTIONAL

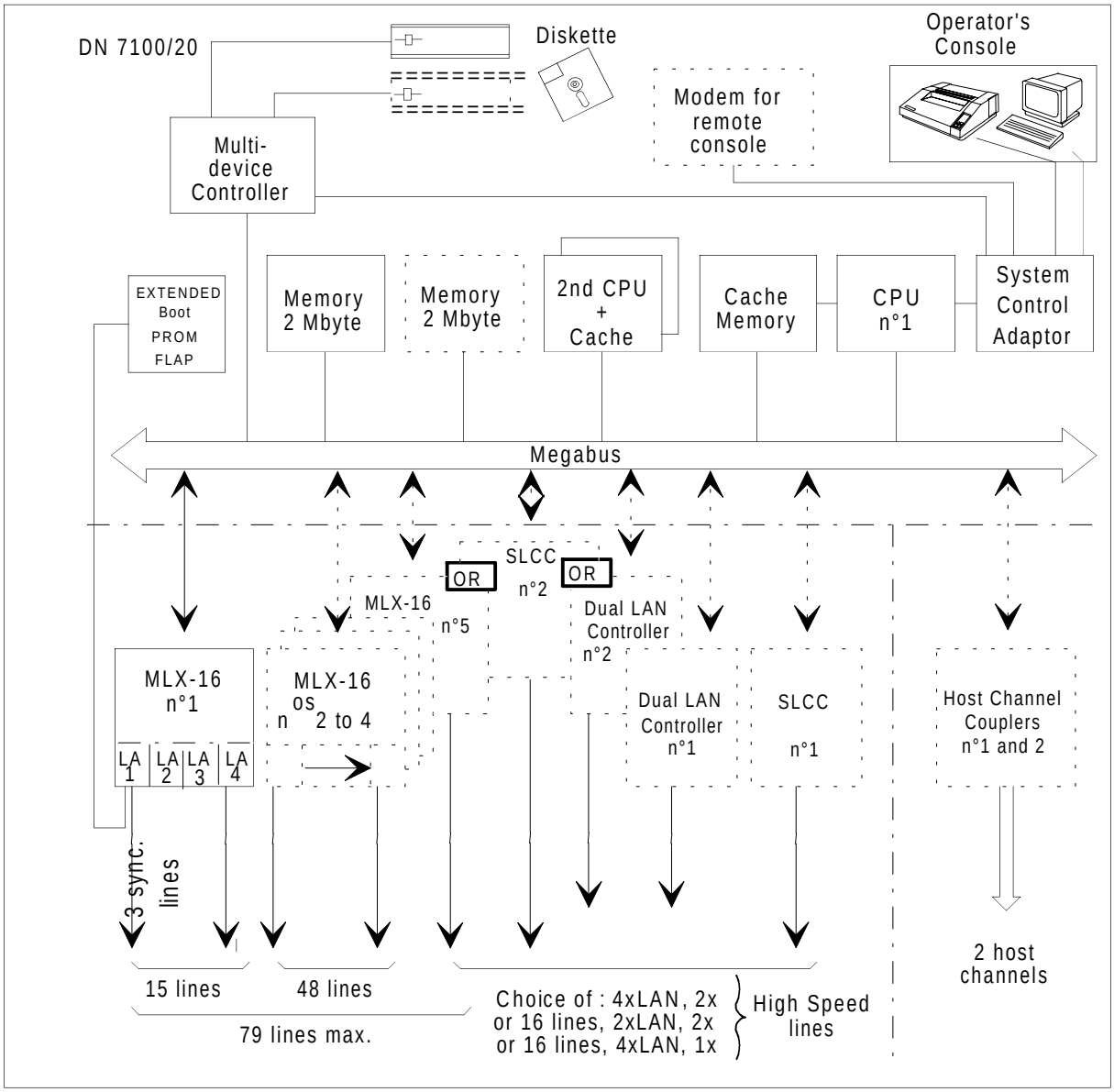


Figure 2-4. DN 7100/20 Configuration

2.4.2 Options

The following equipment may be added to the basic DN 7100/20

- Central subsystem
  - 2 Mbytes memory extension,
  - a second 5,25 inch diskette drive (650K byte).
- Communications subsystem
  - three LA (for sync, async. or HDLC lines) for the standard MLX-16 controller,
  - MLX-16 controllers n° 2, 3, 4 and 5,
  - four LA (for sync, async. or HDLC lines) for each additional MLX-16,
  - Dual LAN controllers n° 1 and 2,
  - SLCC communications controller n° 1,
  - SLCC controller n°2 in place of either MLX-16 n° 5 or Dual LAN controller n°2,
- Host subsystem
  - a second host channel coupler.

2.4.3 Maximum Configuration

Host subsystem

The host systems management of the DN 7100/20 supports a maximum of two host channel connections.

Communications subsystem

The DN 7100/20 can be fitted with a theoretical maximum of 19 optional line adaptors for the MLX-16 controllers.

In addition the DN 7100/20 supports 2 high speed lines via the SLCC and 2 LAN connection, or 1 SLCC and 4 LAN connections.

If 2 High Speed lines (SLCC) and 4 LAN connections are configured, only 4 MLX-16 controllers may be fitted and the maximum number of line adapters is reduced to 15.

This provides the following maximum configurations.

Sync. or Async Lines	HDLC Lines (V.11, V.35, X.21)	HDLC Lines (V.24)	SLCC Connections	LAN Connections
79	0	0	1	4
3	19	0	1	4
3	0	38	1	4
79	0	0	2	2
3	19	0	2	2
3	0	38	2	2
63	0	0	2	4
3	15	0	2	4
3	0	30	2	4

All intermediate combinations are also possible.

As explained in section 3, the theoretical maximum may be reduced by the load factor of the lines used on the MLX-16 controllers.

NOTES:

1. If SLCC(s) are used, the cache memory option is recommended.
2. If the SLCC operates at high speeds, it is recommended to fit the attached processor.
3. In all cases, the installation of an SLCC should be submitted to a Bull Datanet load analysis. For further information, contact your Bull representative.

2.5 MODEL DN 7100/40

For the DN 7100/40, the emphasis has been placed on connectivity and processing power. The system is based on a high performance DUAL central subsystem which uses two 32-bit CPUs in conjunction with an extended memory management unit (EMMU). It is particularly suited as a front-end processor to high power Bull DPS8 mainframes or as a communications processor with high performance switching capabilities and terminal concentration.

The basic model, supplied in two 60 inch high cabinets, can handle up to 127 communications lines. An optional extension cabinet, if fitted, increases the communications capacity to a maximum of 255 lines. Figure 2-5 shows the functional layout of the system.

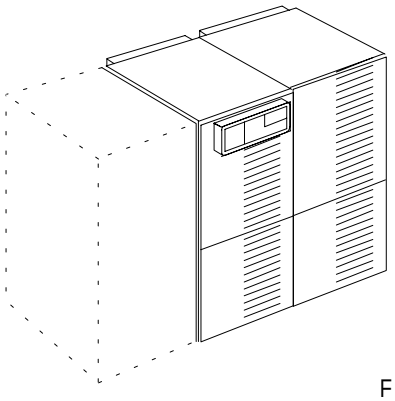
2.5.1 The Basic Machine

The following components are fitted as standard to the DN 7100/40, in two cabinets:

- Central subsystem
  - two CSS chassis, each including CPU, cache, Memory Management Unit,
  - 4 Mbyte of memory,
  - system control adapter board (SCA),
  - Boot PROM FLAP (BPF) for host, diskette and remote loading,
  - Multi-device controller (MDC),
  - one 5,25 inch diskette drive,
- Communications subsystem
  - one MLX-16 communications controller,
  - one LA fitted to the MLX-16. The first line of this LA is fitted with the BPF,

The following components are mandatory add-ons to the DN 7100/40:

- operator's console,
- one host channel coupler (DIA, PSI or CIU) if used as a FEP.

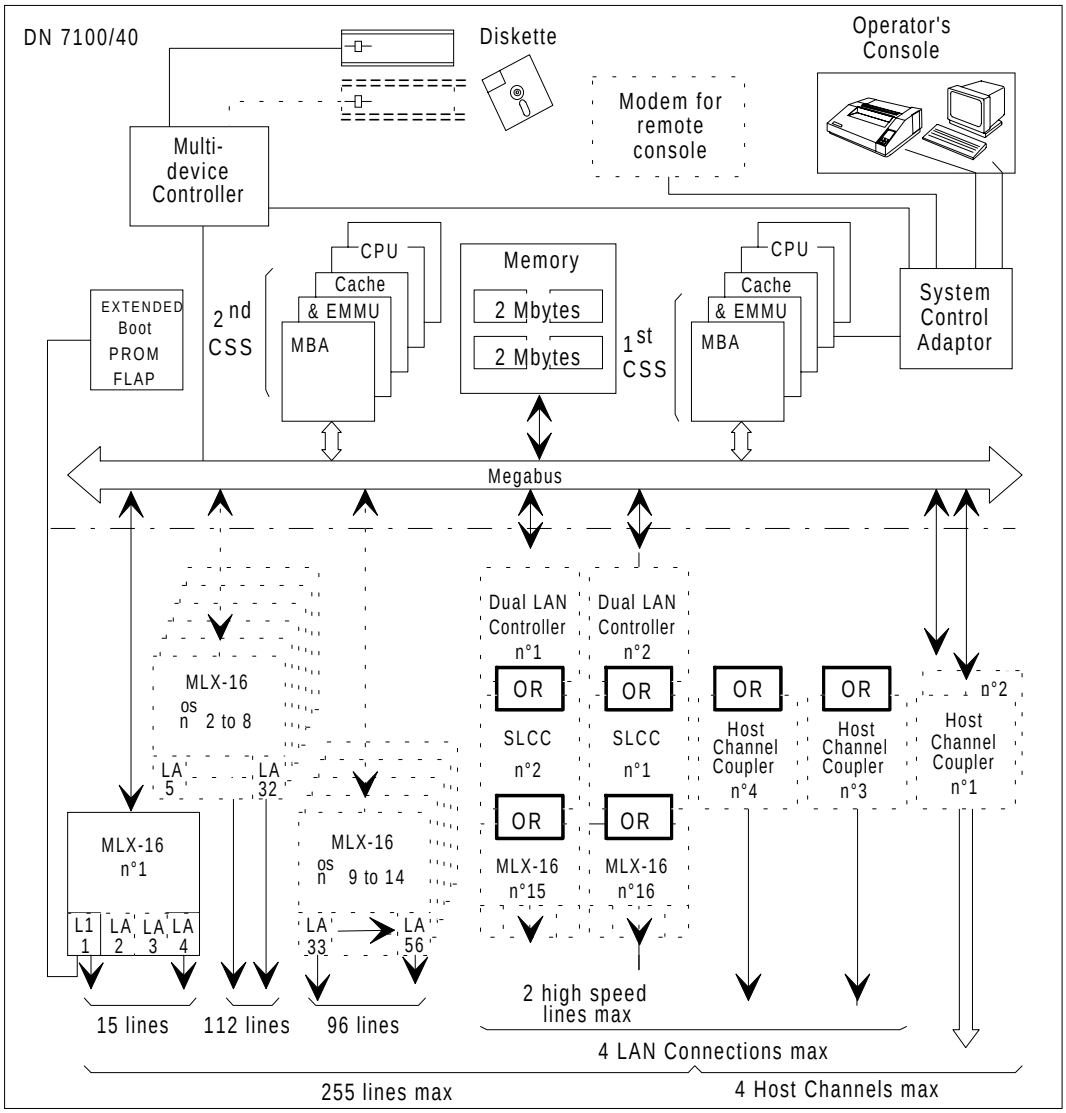


PHYSICAL

= Standard

= Optional

FUNCTIONAL



NOTE: Confuration depends on slot availability - consult the Bull representetive.

Figure 2-5. DN 7100/40 Configuration

2.5.2 Options

2.5.2.1 Two-Cabinet Version

The following optional equipment may be fitted in the two cabinets of the basic DN 7100/40:

- Central subsystem
  - a second 5,25 inch diskette drive,
- Communications subsystem
  - three LA (for sync, async. or HDLC lines) for the standard MLX-16 controller,
  - seven MLX-16 controllers (n° 2 to 8),
  - four LA (for sync, async. or HDLC lines) for each additional MLX-16,
  - SLCC communications controllers n° 1 and 2
  - Dual LAN controllers n° 1 and 2,
- Host subsystem
  - three additional host channel couplers (but with a maximum of two CIU couplers).

2.5.2.2 Three-Cabinet Version

In addition to the options listed above, the following may be added to the DN 7100/40, if it is fitted with the third (extension) cabinet:

- eight MLX-16 controllers (n° 9 to 16),
- four LA (for sync, async. or HDLC lines) for each additional MLX-16.

NOTE: The extension cabinet itself must also be ordered as an optional add-on. It provides the necessary space for connectors and possibly LIU chassis (see section 3) for the additional MLX-16 controllers.

2.5.3 Maximum configuration

- Host subsystem

The host systems management of the DN 7100/40 supports a maximum of four host channel connections.

- Communications subsystem

The maximum number of lines supported by the DN 7100/40 depends on whether the system is fitted with two or three cabinets.

2.5.3.1 Two-Cabinet Version

A theoretical maximum of 31 optional line adapters for the MLX-16 controllers can be fitted. This provides the following maximum configurations:

Sync. or async. lines	HDLC lines (V.11, V.35, X.21)	HDLC lines (V.24)
127	0	0
3	31	0
3	0	62

All intermediate combinations are also possible.

As explained in section 3, the theoretical maximum may be reduced by the load factor of the lines used on the MLX-16 controllers.

The DN 7100/40 also supports 2 high speed lines via SLCC controllers and up to 4 LAN connections via two Dual LAN controllers. These controllers are mutually exclusive either with each other or with two host couplers. This provides the following maximum configurations, which are independent of the MLX-16 configuration:

Host Couplers	Dual LAN Controllers	SLCC Controllers	Total Maximum Host+Dual LAN +SLCC
4	2	0	
4	0	2	
3	2	1	6
3	1	2	
2 (or 1)	2	2	

All intermediate combinations are also possible.

NOTE: The DN 7100/40 configuration must always be submitted to a Bull Datanet load analysis. For further information, contact your Bull representative.

2.5.3.2 Three-Cabinet Version

The DN 7100/40 supports 2 high speed lines via SLCC controllers and 4 LAN connections via two Dual LAN controllers. These controllers are mutually exclusive either with each other or with two host couplers or with two MLX-16 controllers as shown in the following table:

Number of MLX-16	Number of Host couplers	Number of Dual LAN Controllers	Maximum SLCC Controllers	Total Max Host + SLCC + Dual LAN + MLX-16
16	4	0	0	
	3	1	0	
	2 (or 1)	2	0	
		1	0	
15	4	0	1	
		2	0	
	3	1	1	20
	2 (or 1)	2	1	
		2	0	
14 or less	4	0	2	
		2	1	
	3	1	2	
	2 (or 1)	2	2	

A theoretical maximum of 63 optional line adapters for the MLX-16 controllers can be fitted (according to the number of MLX-16 controllers). This provides the following maximum configurations:

No. of MLX-16 controllers	Sync. or async. lines	HDLC lines (V.11, V.35, X.21)	HDLC lines (V.24)
16	255	0	0
	3	63	0
	3	0	126
15	239	0	0
	3	59	0
	3	0	118
14	223	0	0
	3	55	0
	3	0	110

All intermediate combinations are also possible.

As explained in section 3, the theoretical maximum may be reduced by the load factor of the lines used on the MLX-16 controllers.

NOTE: The DN 7100/40 configuration must always be submitted to a Bull Datanet load analysis. For further information, contact your Bull representative.

2.6 PERFORMANCE COMPARISON

Figure 2-6 shows the relative performances of the Bull Datanet range. For CPU performance, the DN 7130 has been taken as the reference (= 1) and the other models are compared with this.

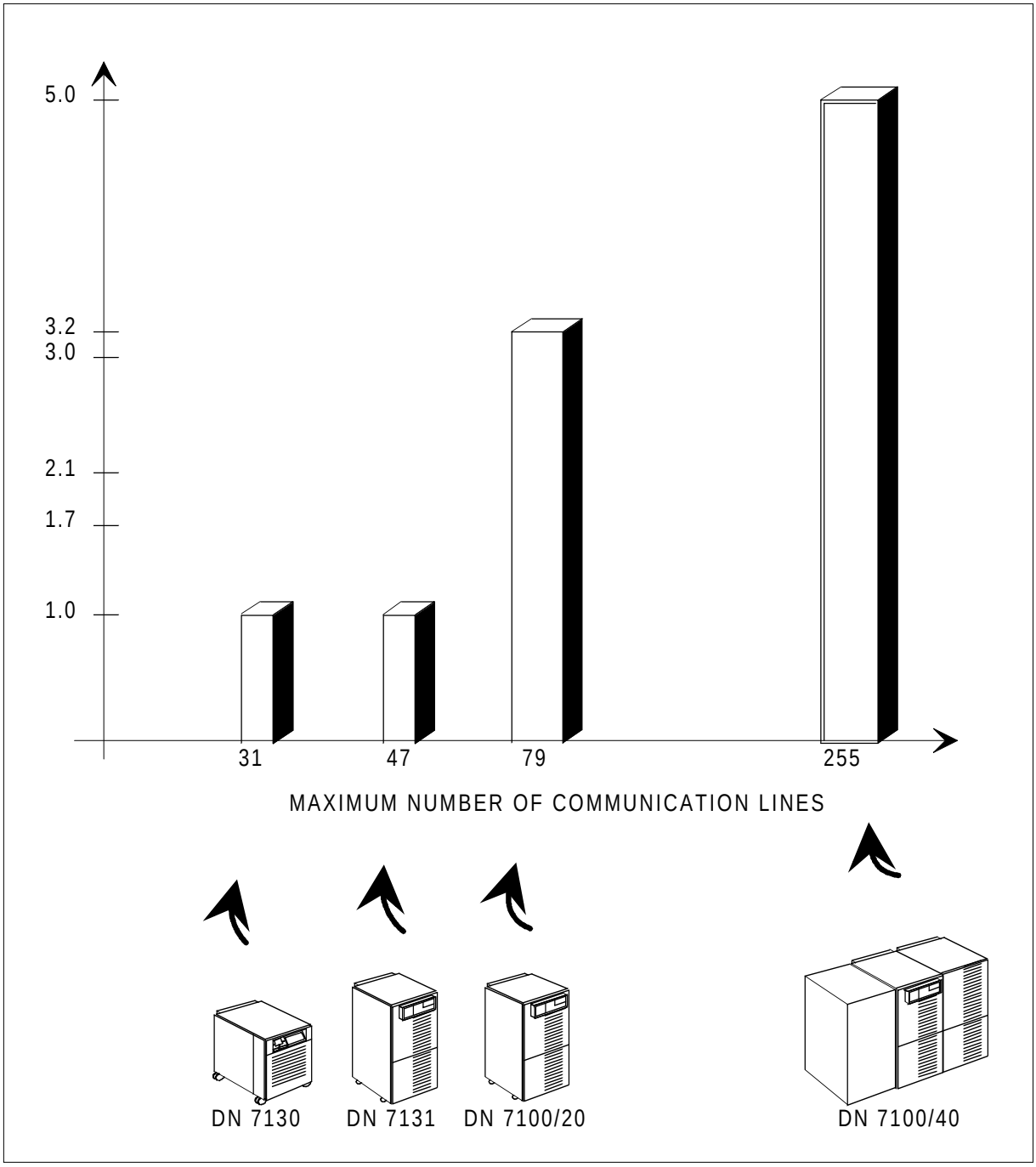


Figure 2-6. Bull Datanet Performance Comparison

2.7 SOFTWARE CONSIDERATIONS

Additional hardware modules require additional software modules to drive them. Thus the DNS operating system is offered as a basic package with optional functions.

The following is a list of the software modules provided with DNS:

- DNS Nucleus
  - Basic DNS without performance extension for model DN 7130,
  - Basic DNS without performance extension for models DN 7131.
  - Basic DNS for models DN 7100/20 and DN 7100/40.
- Host Systems Management
  - 4 modules are offered to support the Bull Datanet FEP function with:

    DPS 8 family of hosts operating on GCOS 8.

    DPS 7 hosts,

    IBM hosts (OSF environment),
- Primary Network Control
  - Interface to OSI/DSA networks,
  - Interface to X.25 private networks,
  - Interface to X.25 public data networks (PDN) including support for PAD and VIDEOPAD facilities,
  - Interface to X.21 PDNs.
  - Interface to ISO 8802.2 and 8802.3 type LAN,
- Open System Facilities (OSF) environment
  - Channel interface to IBM[TM] hosts (local DSA/SNA[TM] gateway),
  - Interface to remote IBM hosts (remote DSA/SNA gateway),
  - OSI access to DSA applications,
  - SNA attached terminals with access to Bull applications,
  - DSA attached terminals with access to IBM applications.
- Secondary Network Control
  - Basic terminal manager (TM) including support of asynchronous terminals,
  - TM extension for VIP terminals,
  - TM extension for BSC 327X terminals,
  - TM extension for BSC 2780/3780 terminals in a DPS 8 environment,
  - TM extension for BSC 2780 terminals in a DPS 7 environment,
  - TM extension for Minitel terminals,
  - TM extension for non-standard terminals,
  - TM extension for SNA 3270 terminals.

[TM] These abbreviations are trademarks of the International Business Machines Company.

- Administration

  - Network Operator Interface (NOI). This is a DSA administrative function. It provides the man-machine interface for a network operator.

The other basic administrative function resident on a Bull Datanet is the Node ADministrator (NAD). This is included in the DNS basic software.

3. Component Descriptions

Each of the three hardware subsystems of the Bull Datanet provides a wide range of functions.

The possibility of connections to several different host processors (including heterogeneous connections), of communications via a whole range of communications lines and management of numerous terminal types make the Bull Datanet an extremely versatile network processor.

Versatility is obtained by providing a range of communications controller types and host couplers. In order to reduce the total number of components, all Datanet models are based on a common hardware set. In addition, certain basic components (communications controllers, for example) can be adapted to suit several environments by simply changing an adapter board.

3.1 GENERAL

The construction of printed circuit boards is based on the principle of a mother board fitted with one or more daughter boards. The mother boards generally plug into the Bull Datanet bus (the Megabus), are microprocessor based and provide common services to the daughter boards.

This technique allows expensive logic components such as error correction circuits or controller microprocessors to be shared by several basic components. It also lends itself to flexibility of system configuration and reductions of:

- cost,
- size,
- electrical power consumption.

3.2 CENTRAL SUBSYSTEM

3.2.1 Megabus

Communications between the components of the Bull Datanet take place via the Megabus. This is a bidirectional, asynchronous bus operating at 6 Mbytes/second (16 bits every 330 nanoseconds). It provides multiplexing for both directions of transfer (input and output) which allows interleaving of the operations of several components at the same time.

Transfers between memory and host or communications controllers are performed using Direct Memory Access (DMA). The CPU is only needed to initialize the transfer which is then executed under control of the controller. Thus I/O operations can occur simultaneously with CPU internal processing.

Each board on the Megabus is assigned a fixed address, a fixed physical location and a predetermined system of connections. This method has the advantages of providing standard basic systems, simplifying system expansion and simplifying maintenance.

Access priority to the Megabus for the boards is specified by hard wired connections in the Datanet. The memory has the highest priority and the CPU the lowest.

The CPU interrupt levels are independent of the Megabus transfer priorities. When the Megabus priority levels are used in an optimum fashion, the interrupt levels allow the most urgent event to be processed first. This approach is particularly suited to the Bull Datanet whose purpose is to coordinate the processing of a wide range of network events.

Physically, the Megabus is implemented on a backplane at the rear of each board chassis. Connectors fitted to the backplane, at each board slot, distribute the bus signals and power supplies to the mother boards installed in the chassis.

The signals printed on this backplane include 32 data bits. Printed circuit boards on the bus only use 16 data bits. These boards are fitted with two Megabus connectors to pick up these signals. 32-bit words are used only for communications between the CPU and memory on the DN 7100/40 model. The Megabus adapter and memory board of this model are fitted with 3 bus connectors.

3.2.2 CSS Implementation

The implementation of the central subsystem depends on the Bull Datanet model.

- Model DN 7l30, and DN 7131.
- These models use the CR41 central subsystem which is a single board comprising CPU, main memory and the SCF.

- Model DN 7100/20

  The central subsystem for these models comprises the 7XE CPU, the main memory and the cache memory. Each of these units is implemented on a discrete board mounted in the main board chassis. The logic for the SCF is also implemented on a discrete board, the System Control Adapter (SCA).

- Model DN 7100/40

  This model uses the 6-9E central subsystem which comprises the CPU and cache memory mounted in a separate CSS chassis. The main memory is implemented on a discrete board in the main board chassis. The logic for the SCF is also implemented on a discrete board, the System Control Adaptor (SCA).

3.2.2.1 Bull DN7130/31 Central Subsystem

The CR41 is the central subsystem (CSS) used on the DN 7130 and DN 7131. By its technology, it provides a cost reduced central processor and minimizes the number of boards required in the Bull Datanet CSS. The CPU, main memory and System Control Facility (SCF) are contained in a single unit (see figure 3-1).

The unit comprises a mother board, plugged into the Megabus, on which are mounted:

- one or two daughter boards (main memory),
- the LSI 6 chip and PROM (CPU and MMU),
- the SCF PROMs,
- the CPU Boot PROM.

Data transfers between the CSS components takes place via a system of busses (see figure 3-5). As shown in the diagram, the memory bus is isolated within the CSS, thus the CPU cannot address any other memory.

Each daughter board contains 1 Mbyte of main memory implemented using 256 kbit chips. Data integrity is ensured by an EDAC system for single bit errors, located on the mother board. The memory is controlled by the memory management unit (MMU) which operates in single fetch mode only but which handles a Long Address Format (LAF). The MMU converts the logical address to the physical address. The LAF configuration has a logical memory address range of 2 Mbytes.

The LSI 6 chip contains the CPU and MMU. It is based on a 16 bit microprocessor and performs the arithmetic, logic and control operations. It operates under control of firmware located on a 4 kword x 56 bit PROM (6 chips).

The 16 bit CPU comprises 18 program addressable registers, including program counter, status registers and data and address registers. The instruction set is compatible with that of the DN 7100/20 and DN 7100/40 models. 64 interrupt levels are provided, as for the top range models, with firmware routines for context saving and restoring.

The CPU Boot PROM contains the Quality Logic Tests (QLT) for the CPU and memory and also the bootstrap loading routines.

The SCF is contained in two PROMs on the mother board. Its functions are described later on in this section.

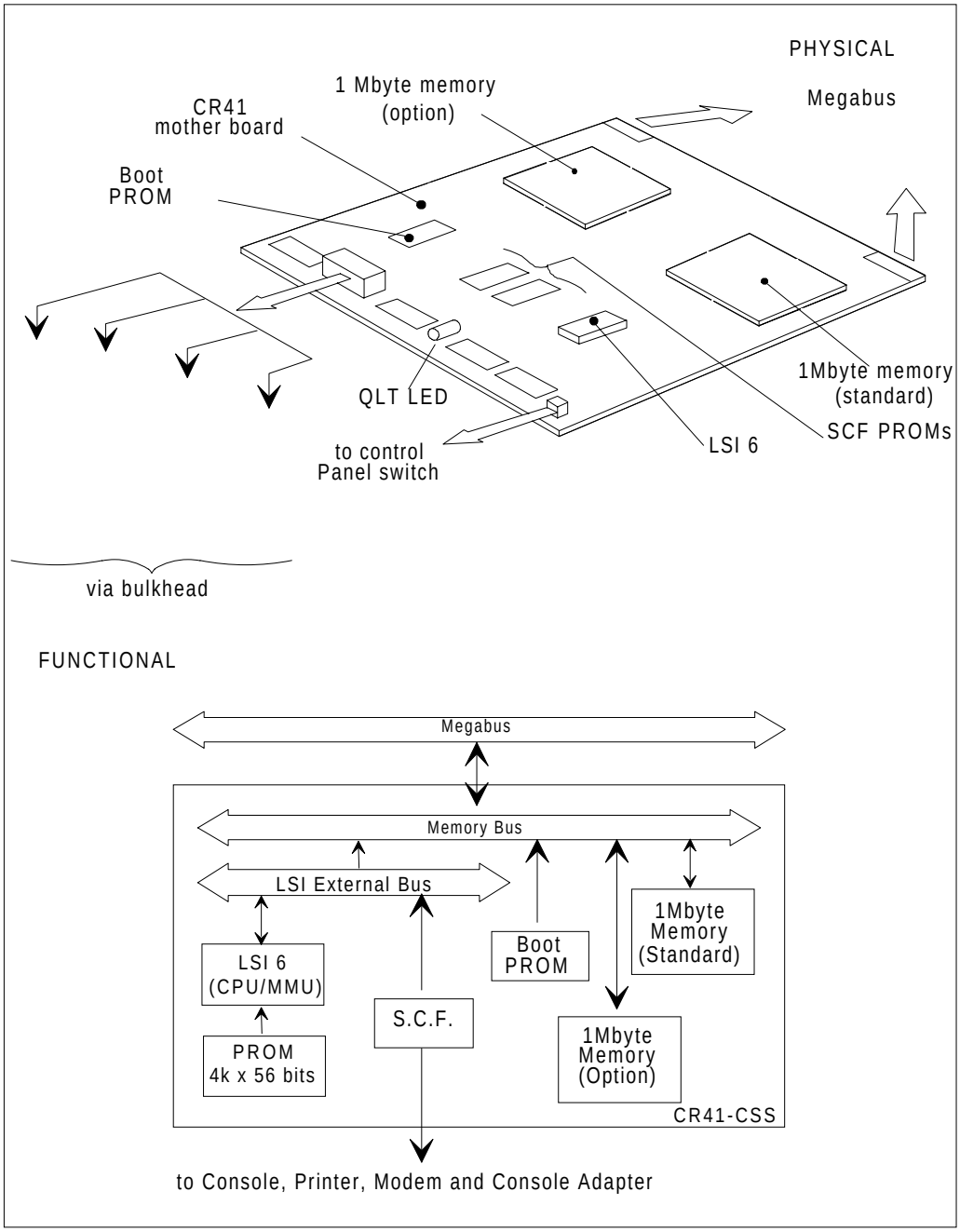


Figure 3-1. Bull DN7130/31 Central Subsystem

Communications between the CR41 and its environment are made via two ports on the mother board. YO4 provides the interface with the local and remote consoles, an auxiliary device (the printer) and the console adapter on the MDC board. YO1 provides the connection to the system control panel mounted on the front of the Bull Datanet cabinet.

3.2.2.2 The Bull DN 7100/20 Central Processor Unit

The DN7100/20 comprises two CPUs. Each CPU is a 16-bit processor with 26 internal program addressable registers including program counter, status registers and data and address registers.

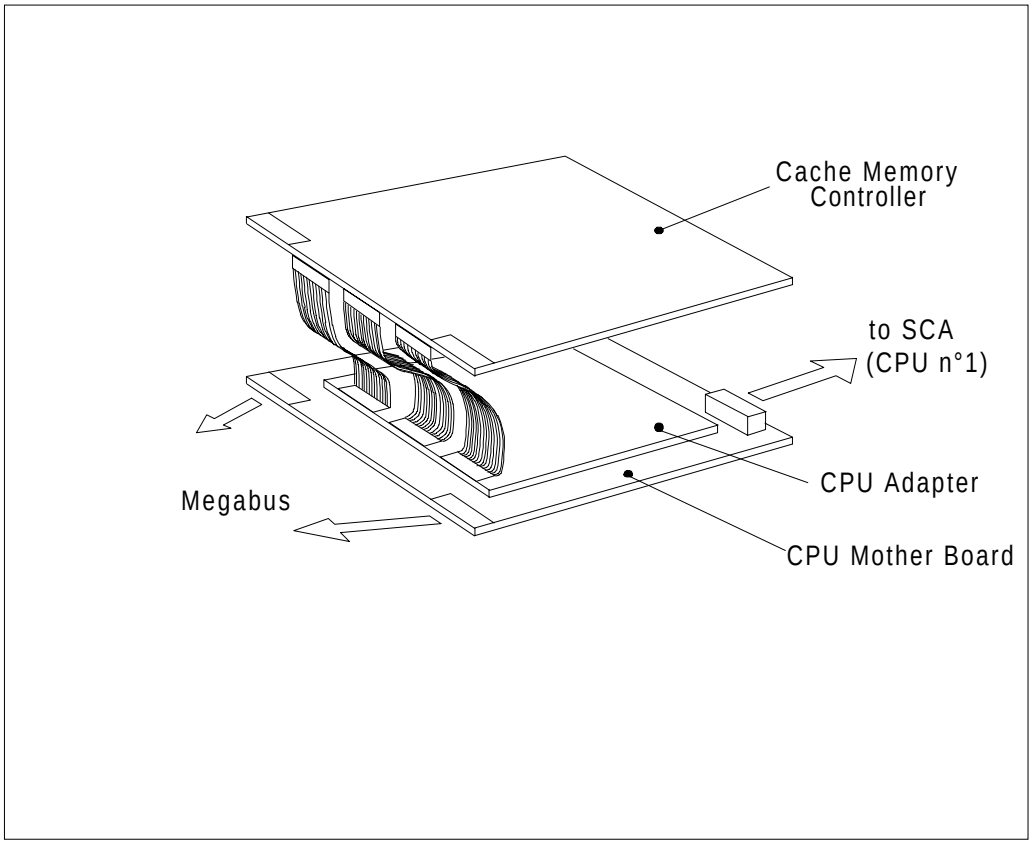


Figure 3-2. The Bull DN 7100/20 CPU and Cache Memory

The 124 instruction set includes: instructions operating at bit, byte and word level; facilities for flag setting, masking and testing; and stack and queue instructions. Register to register and register to memory operations are also offered. 64 vectored interrupt levels are provided. Trap and interrupt routines and automatic context saving and recovery are under firmware control.

The CPU comprises a mother board fitted with a single daughter board, the CPU adapter (figure 3-2). The CPU adapter contains the memory management logic for the cache memory It is fitted with three connectors which provide the interface with the cache board (if fitted).

3.2.2.3 Cache Memory

The purpose of the "cache" memory (also known as the "Performance Extension") is to reduce memory access time and thus increase CPU processing power. The mother board is fitted with 4 kwords of RAM. Being cabled directly to the CPU (see figure 3-2), its cycle time is considerably reduced compared to the Bull Datanet main memory (110 nanoseconds compared to approx. 600 ns).

Each time the CPU fetches data from memory, it checks first to see if the data is already present in the cache. If so, the CPU fetches the data directly from the cache, without referring to main memory. Algorithms are used to maximize the probability of working data being present in the cache.

3.2.2.4 The Bull DN 7100/40 Central Subsystem

The subsystem used on the DN 7100/40 comprises the following components (see figure 3-3):

Two 32-bit CPU mounted in two CSS chassis.

Each CSS comprises:

- CPU complex (Mother + Daughter) boards.
- Megabus Adapter board (MBA) installed on the Megabus.
- Cache Complex (Mother + Daughter) boards.
- Memory board installed on the Megabus (not shown in the diagram).

Each of the two units in an CSS chassis comprises a mother board fitted with a single daughter board. The mother board is connected to its daughter board via a "side hat" connector. The mother board plus daughter board plus side hat connector form a complete assembly which is removed or installed as a single unit.

The CPU and cache memory communicate with each other, and with the rest of the system, via the CSS local bus implemented on the side of the chassis. Unused slots of this bus are fitted with "cheater" boards. A small interface card fitted to the CPU provides the link to the SCF.

The cache memory (mother board plus daughter board) together with the Megabus Adapter form the cache complex which performs the following functions:

- Megabus management,
- CSS local bus management,
- cache memory,
- Extended Memory Management Unit (EMMU) necessary for addressing above 2 Mbytes.

The MBA is connected to the Megabus via three connectors (32-bit words) and to the CSS chassis via 8 ribbon cables (only 4 are shown in the diagram). It provides the interface between the Megabus and the CSS local bus.

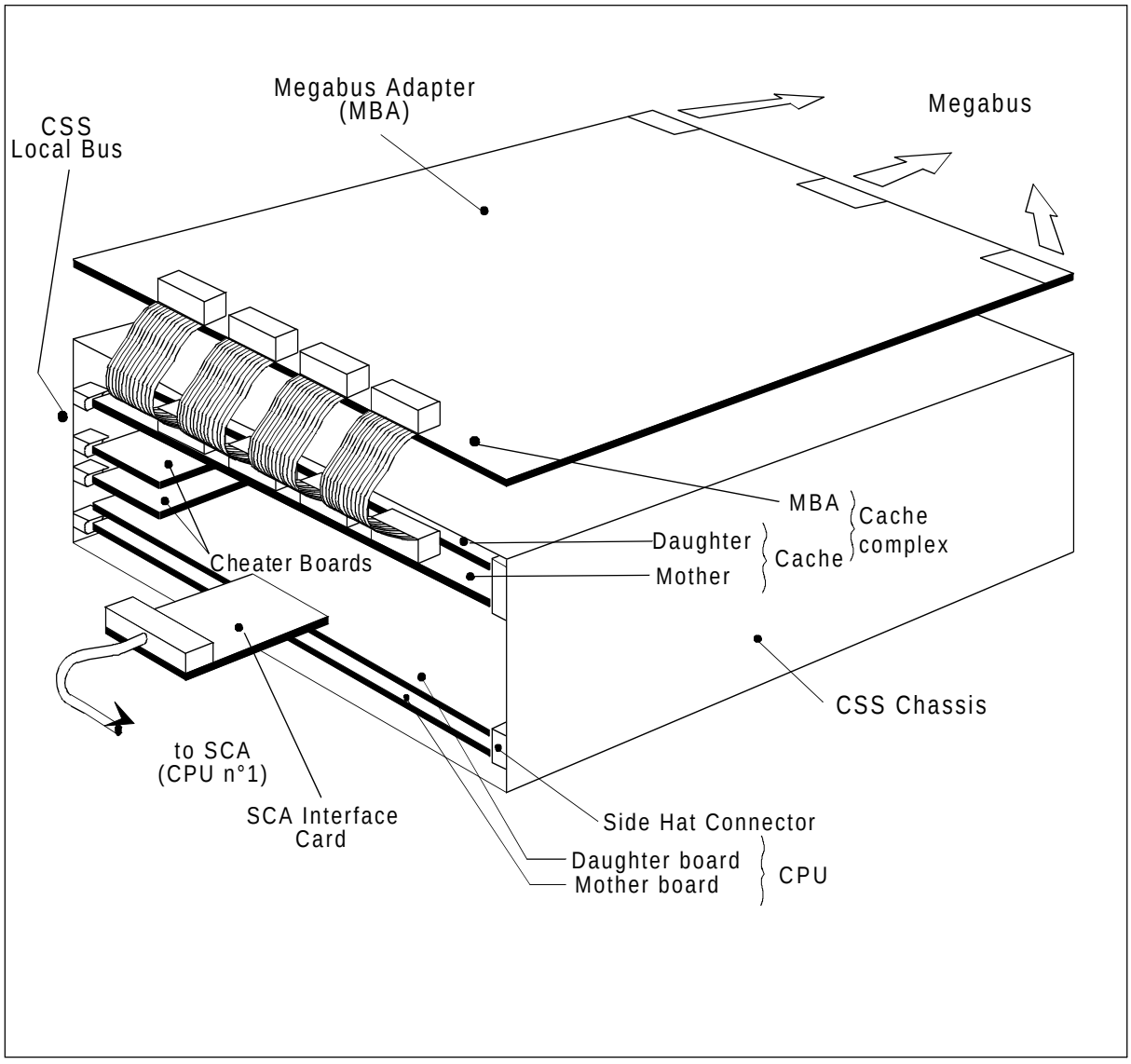


Figure 3-3. The Bull DN 7100/40 Central Subsystem

3.2.2.5 Memory Board

Discrete memory boards comprise a mother board (memory controller) fitted with one or more daughter boards (memory Pac(s)), as shown in figure 3-4.

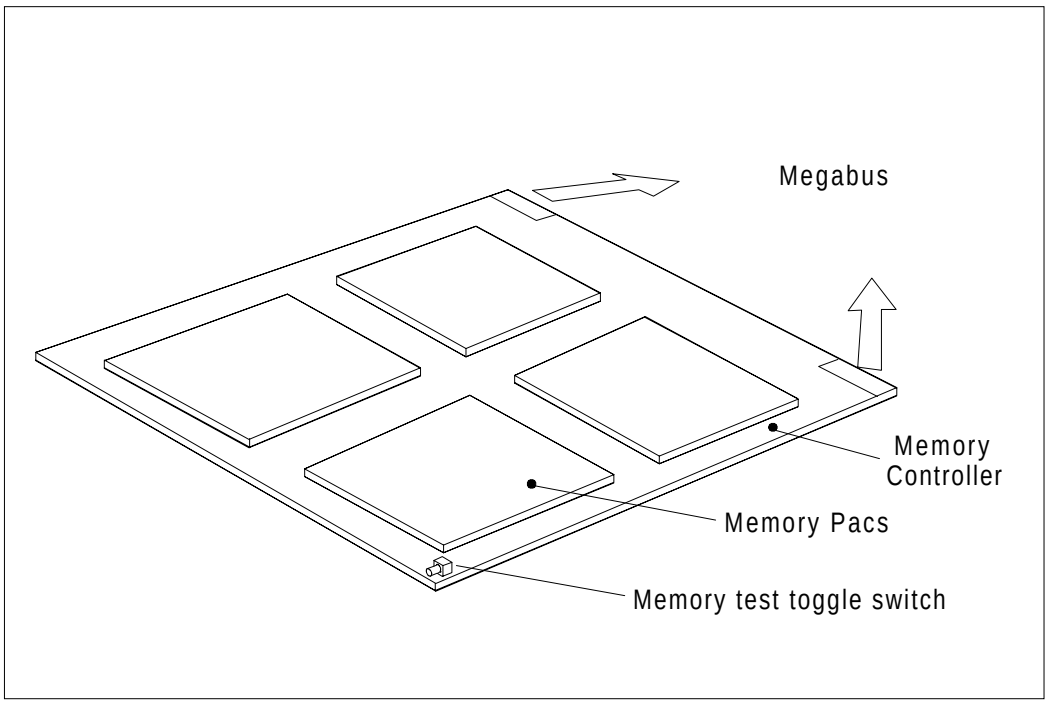


Figure 3-4. Memory Board

The memory Pac(s) contain the RAM chips while the mother board provides the following common services:

- Error Detection And Correction (EDAC) for single bit errors,
- Memory Management Unit (MMU),
- Megabus access and interface logic,
- memory refresh and initialisation logic.

The memory controller uses two-way interleaving, thus the reading of double words (double fetch) is possible which reduces the average memory access time.

3.2.3 System Control Facility

The user's interface with the Bull Datanet is the operator's console. It comprises a screen, keyboard and hardcopy printer (see later). The operator's console and associated control logic form the System Control Facility (SCF).

The SCF replaces the maintenance panel (the Full Control Panel) which was fitted to earlier models of the Bull Datanet. It allows the user to communicate directly with the Datanet CPU and with the DNS operating system. It can be divided into two functional parts:

- System Control Panel (SCP) mounted on the front of the Datanet cabinet. It comprises the mains ON/OFF switch and the PANEL SECURITY key,
- Virtual Control Panel (VCP) which is responsible for the execution of control panel functions, display of status information, etc,

In addition, the SCF includes a remote console port, used for remote monitoring and tele-maintenance. According to the SCF mode selected by the user, the remote console may have control of the Datanet or may simply duplicate the information displayed at the local console.

3.2.3.1 SCF Hardware

The SCF hardware includes the following (see figure 3-5):

- system control panel (SCP),
- operator's console,
- console adapter fitted to the MDC board,
- SCF logic,
- remote console port.

These components are common to all Bull Datanet models. However the implementation of the SCF logic differs according to the type of CPU used. For models using the CR41 CSS the SCF logic is implemented in two PROMs on the CR41 board (see figure 3-1). For other models (using CPUs with discrete boards) this logic is implemented on the System Control Adapter board (see figure 3-6).

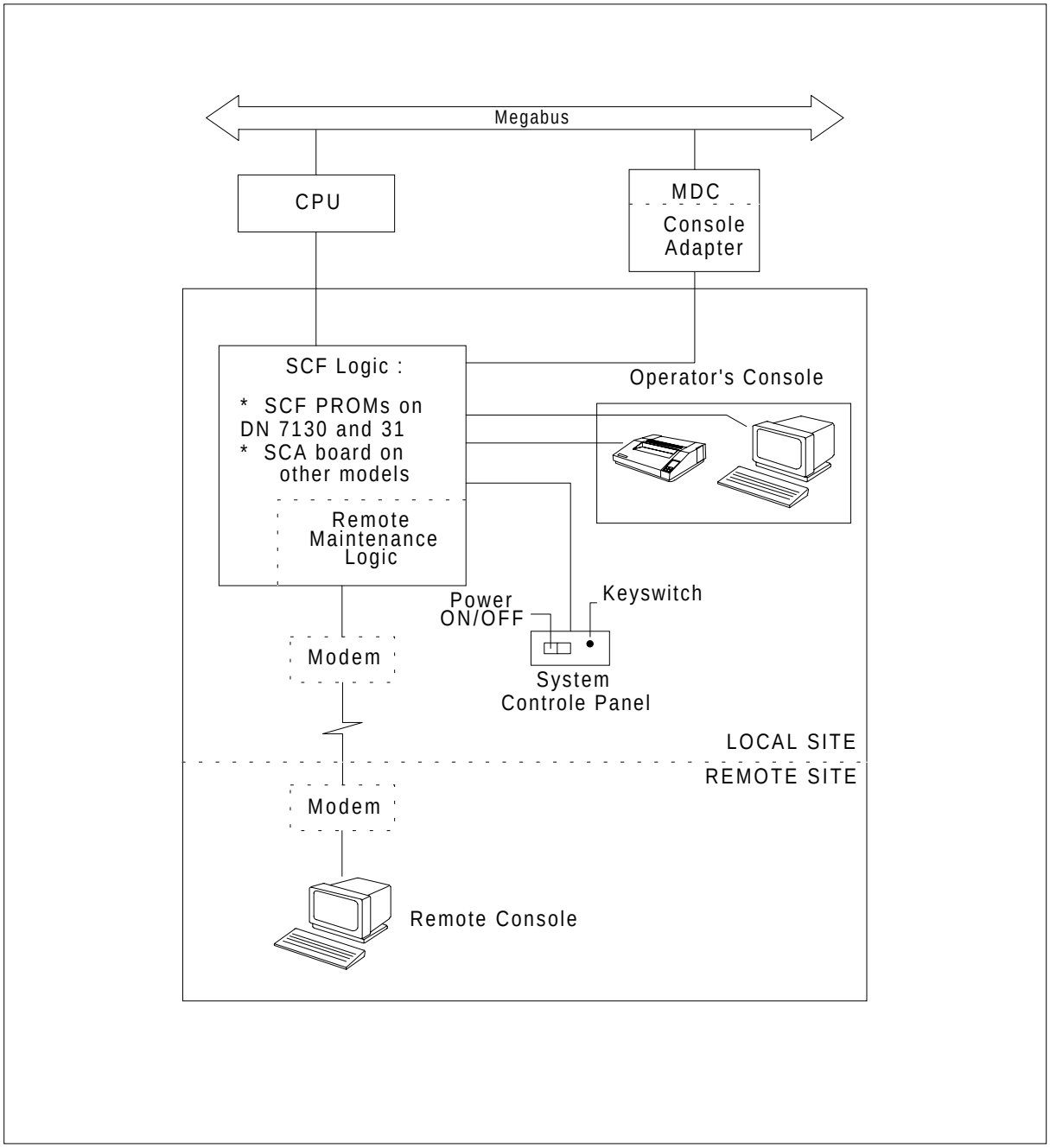


Figure 3-5. SCF Configuration

The SCF does not use the Megabus to communicate with the rest of the system. The SCF of the CR41 CSS communicates via the LSI 6 external bus and the ports on the CR41 board. The SCF based on a separate SCA board communicates via cables connected to the SCA board.

In order to dialogue with the operator interface routines of the Datanet software, the SCF must include a program addressable hardware component installed on the Megabus. This is the purpose of the console adapter fitted to the MDC board.

3.2.3.2 System Control Adapter

The System Control Adapter (SCA) contains the logic for the SCF. Microprocessor based, it is the only board which does not communicate via the Megabus. Megabus connectors on the board are used only to pick up power supplies. It communicates directly with its environment (CPU, console, etc.) via cables (see figure 3-6).

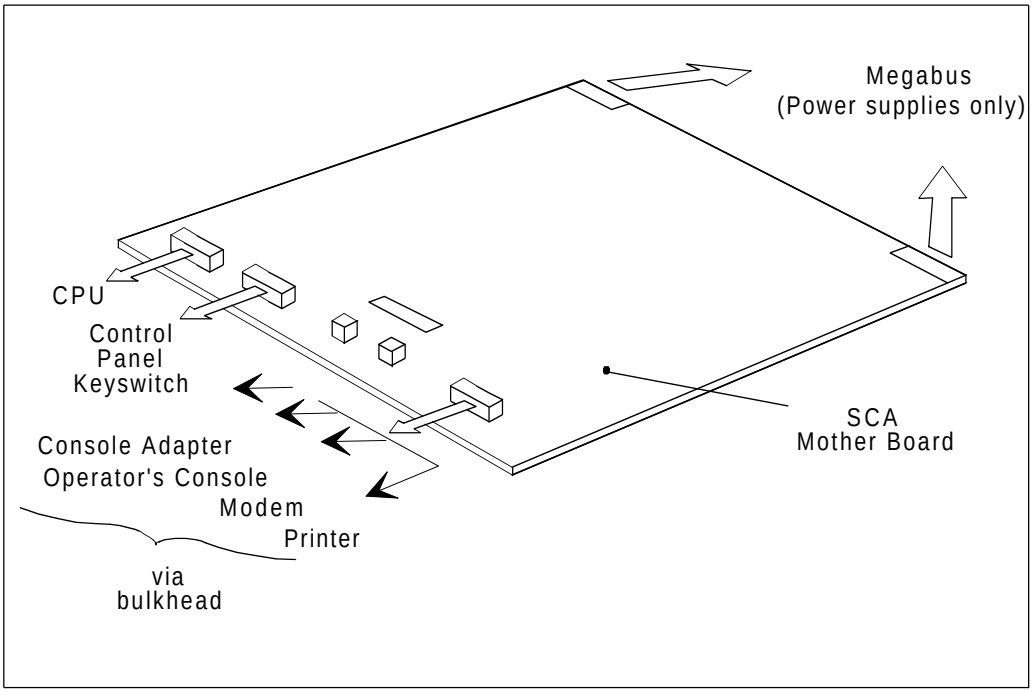


Figure 3-6. System Control Adapter Board

3.2.3.3 Virtual Control Panel

On previous models of the Bull Datanet, status information was displayed on the maintenance panel (Full Control Panel). On the DN 713X range of Datanets this information is displayed on the 25th line (bottom line) of the operator's console, or on the next sequential line of the printer. This display is managed by a function of the SCF called the Virtual Control Panel (VCP).

The VCP performs a subset of the SCF functions. These include:

- execution of control panel functions,
- status indications (on the 25th line),
- commands and messages to the operator,
- local and remote display of maintenance information,

- V.24/RS 232 interface for the local and remote consoles,
- interface for the printer.

Control panel functions are entered using specific keys at the keyboard (function keys or standard keys according to the SCF mode selected). They are available at both the local and remote consoles.

3.2.3.4 SCF Functions

The functions performed by the SCF depend on the selected state and mode. The SCF can operate in two distinct states; Normal State and Remote State.

In the Normal State the local control panel and local console operations between the SCF and the CSS are enabled. Remote console operations are disabled.

In the Remote State the remote maintenance operations of the CSS are enabled, together with local console functions. Two operators (one local and one remote) interface the system, though as far as the system is concerned, only one operator exists. The SCF ensures that only one console is in control at any given time. The operators are informed which console is in control by information on the 25th line.

The SCF can operate in the following mutually exclusive modes:

- Console Mode,
- Panel Mode (Normal State only),
- Maintenance Mode (Remote State only),
- Text Mode (Remote State only),
- Command Mode,
- Dump Mode,
- Self Test Mode.

All these modes are available in either of the SCF states, except where mentioned above.

Console Mode

In this mode the local or remote console operates as an ordinary terminal connected to the Bull Datanet. The operator can perform all standard functions supported by the operating system. The operator can access the Datanet NOI from this console but he cannot access other Datanet resident applications.

Control panel status information is not displayed on the 25th line unless specifically requested. Operator messages are transmitted to the operating system and system messages are transmitted to the console (via the console adapter on the MDC).

Panel Mode

In this mode the local console operates as a maintenance panel. It is only possible to use this mode when the SCF is in the Normal state.

Control panel functions (such as Master Clear, Load, Execute, Step, etc.) are entered using specific function keys. Control panel status information is displayed on the 25th line of the console. The operator's input is not displayed but the corresponding status information is updated automatically as soon as the key is pressed.

System messages are displayed on the console (except on the 25th line) but no data is sent from the console to the operating system.

Maintenance Mode

In this mode the control panel functions are available to both a local and a remote operator. Also, the operator's input is displayed on the 25th line. Status information at the remote console is updated only after entering <CR>.

There is no transmission of messages either to or from the operating system.

Text Mode

This mode is used for exchanging messages between the local and remote operators. The console screen is cleared on entry into the Text mode and then all messages input are simultaneously displayed at both consoles in the main part of the screen (lines 1 to 24).

The control panel commands are not available and there is no transmission of messages either to or from the operating system.

Command Mode

This is an intermediary mode between other SCF modes. It is used to direct the SCF to another mode.

The operator can enter the Command mode from any other mode and can then scan a menu of other modes available. The menu is displayed, one mode at a time, on the 25th line by pressing the # key. The operator selects the displayed mode by pressing the ENT (enter) key.

Dump mode

This mode is used for displaying CPU register contents or memory contents or for starting the Quality Logic Tests (QLT). Four functions are available:

- Dump Register Contents. The contents of the CPU registers are displayed,
- Dump Memory Contents. The memory image is displayed starting from a user specified start address up to 184 memory locations (23 screen lines),
- Dump Found Memory Match. The SCF searches in main memory for a specified memory contents and displays the address of each match found. The process continues to one screen full. The operator then has the choice to continue or to terminate,
- Reset and Start QLTs. The SCF performs a general reset (and on the CR41 CSS initiates the Quality Logic Tests).

Self Test Mode

After power on of a Bull Datanet, the SCF automatically enters the Self Test mode. At the end of the tests the SCF enters either the Panel mode (if the control panel is unlocked) or the Console mode (if the control panel is locked).

3.2.3.5 System Control Panel

The system control panel of the DN 71XX is a reduced size panel mounted at the front of the cabinet, containing only two controls (see figure 3-5):

- ON/OFF power switch,
- PANEL SECURITY keyswitch.

The ON/OFF switch controls the a.c. mains input supply to the system.

In the LOCK position (anti-clockwise) the keyswitch inhibits control panel functions and forces the system to be booted from a predetermined address at power on.

In the UNLOCK position (clockwise) the keyswitch enables the control panel functions via the VCP facility.

3.2.3.6 Boot Prom Flap

At power on, the Bull Datanet is inoperable since it contains no software. Each Datanet is therefore provided with sufficient firmware to load the operating system. This is located in a PROM on the Boot PROM FLAP (BPF).

Although the BPF is part of the Datanet central subsystem, it is connected to the standard MLX-16 communications controller provided with each system. It is therefore described later on in this section.

3.2.4 Operator's Console

The DN 7100/XX series must be fitted with an operator's console. It comprises:

- screen,
- keyboard,
- hardcopy printer.

The console is connected to the Bull Datanet via the SCF and provides the operator with access to the Datanet internal operation.

3.2.5 Diskette and MDC

Each Datanet is fitted with a single diskette drive as standard. The drive accepts 5,25 inch diskettes and provides a storage capacity of 640 kbytes.

The diskette drive operates under control of the Multi-Device Controller (MDC III). The MDC is a general purpose controller comprising a mother board fitted with one or more daughter boards (device adapters). The motherboard includes the microprocessor with 2 kbytes of ROM.

The device adapters have 64 bytes of internal memory used for I/O operations and provide the specific interface with the device. All DATANET models are equipped as standard with an MDC fitted with two device adapters (see figure 3-7):

- diskette adapter,

- console adapter (see paragraph "SCF Hardware").

All models may optionally be fitted with a second diskette drive, mounted on the front panel of the cabinet. This unit is interfaced to the system via a second diskette adapter mounted on the MDC controller.

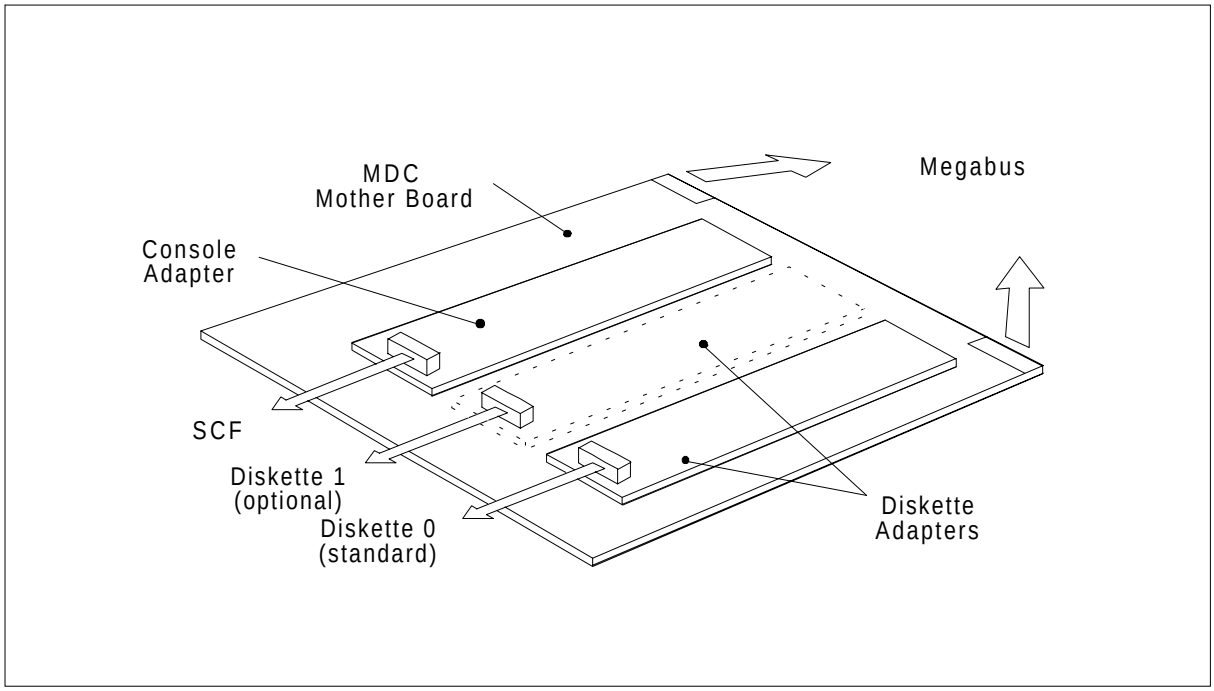


Figure 3-7. Multi-Device Controller

3.3 COMMUNICATIONS SUBSYSTEM

The Bull Datanet communications subsystem comprises three types of communications controllers:

- supporting async, sync. or HDLC lines at speeds up to 64 kbit/s over a wide range of network types, line protocols and electrical interfaces,
- SLCC supporting HDLC links using the LAP.B procedure at speeds up to 64 kbit/s over V.35 interfaces and 2 Mbit/s over X.21 interfaces,
- Dual LAN controller supporting ISO 8802.2 and 8802.3 type local area networks at speeds from 1 Mbit/s to 10 Mbit/s.

Connections from these boards to the communications lines are made via the bulkhead at the rear of the system cabinet or from the rear of the LIU chassis (for certain connections to the MLX-16 controller).

3.3.1 Multi-line Controller (MLX-16)

The MLX-16 Multi-line controller is the main communications controller of Bull's DATANET processors. It is a programmable controller which supports up to 16 lines of the primary and secondary network.

Physically, the MLX-16 comprises a mother board fitted with one or more daughter boards, called line adapters (see figure 3-8).

3.3.1.1 MLX-16 Mother Board

The mother board is microprocessor based and performs the common services, including the interface with the Megabus, command decoding and data exchange with main memory using DMA. It also performs CRC error checking for all channels.

Data is transferred between main memory and each line adapter. Each character is handled individually by the MLX-16 microprocessor. A combination of firmware (resident on the MLX-16) and software (Channel Control Programs) is used to process each data element.

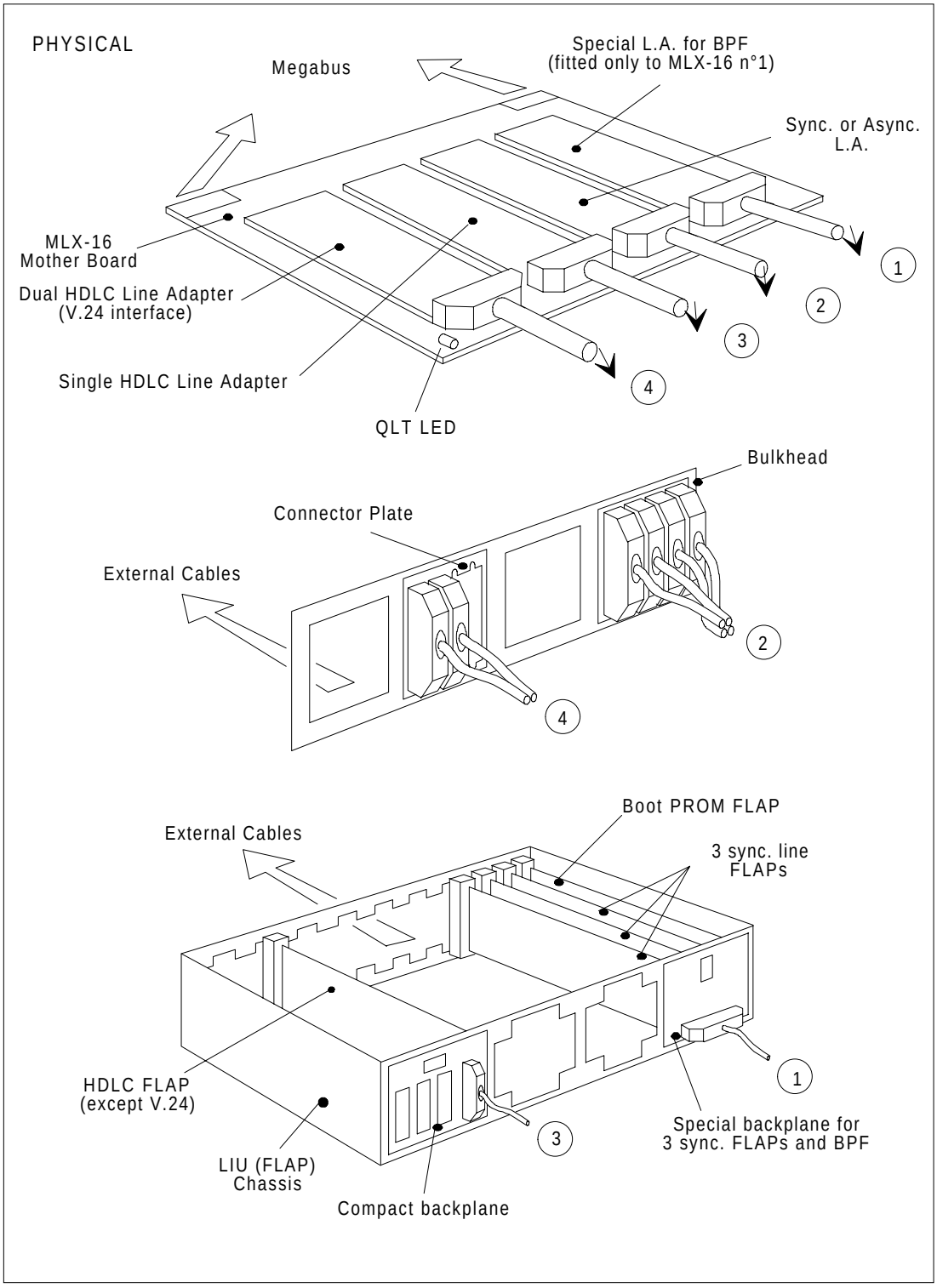


Figure 3-8. MLX-16. Communications Controller (1/2)

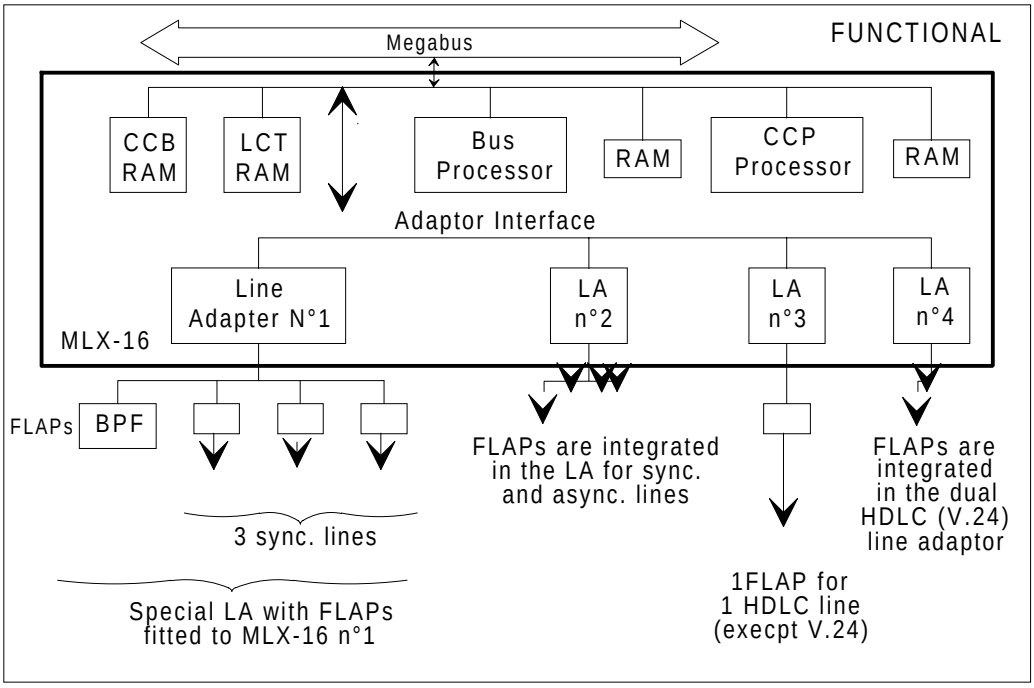


Figure 3-9. MLX-16 Communications Controller (2/2)

As shown in the diagram, the mother board supports up to 4 line adapters. Each line adapter supports:

- either 4 synchronous or asynchronous lines,
- or 2 HDLC lines via a V.24 interface,
- or 1 HDLC line via a V.11, V.35 or X.21 interface.

The maximum number of lines is thus 16 per controller.
Due to the microprocessor scanner, the line adapters must be fitted in the correct priority order, as follows:

- Synchronous - lowest address,
- Asynchronous,
- HDLC (V.24),
- HDLC (V.11, V.35, X.21) - highest address.

3.3.1.2 Line Adapters

The line adapters (LA) perform the specific services including serial/parallel conversion of data, character buffering and support of the line procedures for the various types of communications lines.

Adapters are of two types:

- integrated adapters which are connected directly via bulkheads to the lines they support (for all sync. and async. line adapters and for the dual HDLC/V.24 line adapter),
- adapters connected through Line Interface Units (for single line HDLC adapters). The LIUs are mounted in an LIU chassis, the rear side of which comprises connectors for the communications lines.

3.3.1.3 Line Adapter Types

Seven types of adapter are currently available as indicated in table 3-1.

The maximum number and the type of adapters that can be connected to one MLX-16 depend on the load factors, given in table 3-2.

Each line of a 4-line LA (for sync. or async. lines) can be separately configured for speed and data format.

For modem connections, the modem cable is supplied with the line adapter. When using a type 5 line adapter on French PTT networks (Transpac, Transfix, Transcom or Transdyn), a connector adapter must be fitted to the modem end of this cable.

One type of line adapter not shown in table 3-1 is the line adapter fitted as standard to the first MLX-16 of all DN 71XX models. This is a specific adapter used to connect the Boot PROM FLAP and 3 synchronous V.24 lines.

Table 3-1. Line Adapters Currently Available

Type n°	No. of lines	line procedure and max. speed	Electrical interface
Integrated adapters:			
0	4	asynchronous, direct connection, half or full duplex, 19.2 kbit/s	V.11/RS 422
1	4	sync, modem or direct connection, half duplex, 19.2 kbit/s, VIP or BSC	V.24/RS 232C
2	4	async, modem or direct connection, half or full duplex, 19.2 kbit/s, start-stop	V.24/RS 232C
Adapters connected through LIUs:			
5	1	HDLC, modem or direct connection, full duplex, 64 kbit/s, packet networks or OSI/DSA nodes	V.35
6	1	HDLC, modem connection, full duplex, 64 kbit/s, circuit switching networks	X.21
7	1	HDLC, direct connection, full duplex, 19.2 kbit/s, OSI/DSA nodes	V.11/RS 422
Integrated Adapter:			
8	2	HDLC, modem or direct connection, full duplex, 19.2 kbit/s, packet networks or OSI/DSA nodes	V.24/RS 232C

Table 3-2. Load Factors for MLX-16 Lines

Line Type and Interface	Line Speed (kbit/s)					
	4.8	9.6	19.2	48	56	64
Async V.11, V.24:						
-no echo or t.a.	3.1	6.2	12.3	-	-	-
-echoplex	3.7	7.4	14.8	-	-	-
-type ahead	5.9	11.7	23.4	-	-	-
-echo + t.a.	6.5	13.0	25.9	-	-	-
Synchronous: V.24	3.4	6.8	13.6	-	-	-
HDLC:						
V.11 V.24 V.35	4.1	8.2	16.3	40.6	47.4	54.0
X.21	5.8	11.7	23.4	58.5	68.2	77.9

Notes:
1. The sum of the load factors for each controller must not exceed .
2. The load factors for lower speeds, not shown in this table, are lower in proportion to the speed.
3. The line adapters for sync. and async. lines and the dual HDLC/V.24 adapter can handle more than one line. All lines used must be included in the calculation of load factor.

3.3.1.4 Line Interface Units

The line interface unit (LIU) provides the mechanical and electrical interface to the DCE. It is a configurable hardware package connected to the line adapter and is therefore also called a FLAP (Flexible Line Adapter Package). It should be noted that LIUs are only required for single line HDLC adapters and for the special line adapter fitted with the Boot PROM FLAP.

The existing range of LIUs for HDLC adapters includes the following interfaces:

- V 24/RS 232C
- V.11/RS 422
- V.35
- X.21

LIUs (or FLAPs) are mounted in an internal chassis (the LIU chassis). They are cabled to their line adapters at the front of this chassis and to the modems or direct connections at the rear.

3.3.1.5 Boot Prom Flap

The Boot PROM FLAP (BPF) is fitted to all DN 71XX models. It replaces the functions of the Main Memory PROM Option (MMPO) of earlier Bull Datanet models. Its name is a resume of its key features:

Boot	It provides the bootstrap firmware which loads or dumps the Datanet operating system,
PROM	The standard unit is fitted with an erasable PROM which contains the firmware for host or diskette loading. The optional BPF is fitted with an extended PROM for diskette and host loading and for tele-loading via an HDLC line or a local area network.
FLAP	Flexible Line Adapter Package (or LIU as mentioned previously). It is flexible in the sense that it adapts the LA to the required functions; load/dump and unbundling. It is a line adapter package because it is connected to the special line adapter fitted as standard to all DN 71XX models.

The BPF is connected to the first line position of the special line adapter of MLX-16 n° 1 (figure 3-8). The board occupies one slot of the LIU chassis. It should be noted that because of the BPF, MLX-16 n° 1 supports a maximum of 15 lines instead of 16.

The main components on the board are shown in figure 3-9:

- one EPROM,
- 16 switches for load path selection,
- 16 switches for unbundling control.

Each group of 4 load path switches corresponds to one load path address, i.e. the Megabus address of one hardware component via which the memory image may be loaded or dumped. These may be:

- a diskette drive (local loading),
- a host channel (host loading),
- an HDLC line (tele-loading),
- a LAN connection (tele-loading).

Hardware tables are used to convert the 4 bit code selected with the switches to the 16 bit address of the load path.

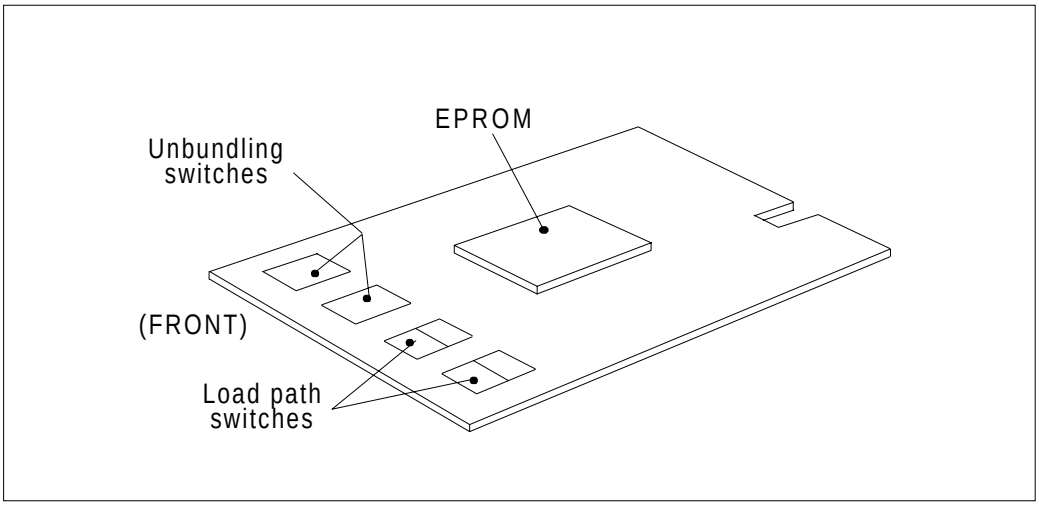


Figure 3-10. Boot PROM FLAP Board

At power on, the contents of the BPF PROM are loaded into the Datanet main memory by the initial boot routine contained in the CPU Boot PROM of the system control facility. The BPF software then scans the four loading addresses in sequence and tries to initialize the load/dump process from the first operational address. If it is not possible to load from this address the BPF routine tries again at the next address. Having unsuccessfully scanned all the addresses, the BPF starts again from the first.

The unbundling switches are used during DNS system generation. They permit the appropriate DNS modules to be generated according to the specific configuration of the system. They are used in conjunction with the 44 character encoded-options-string which defines the options of a system for a given user.

A Watchdog Survey Facility has also been implemented, not on the BPF but on the channel associated with the BPF on the MLX-16 mother board. The facility includes a timer which is regularly reinitialized by the operating system. The time out value is selected at system generation and may be up to 6 seconds. If the software fails to reinitialise the timer (e.g. due to a loop condition) the timer decrements to zero and sends an interrupt to the CPU. The CCP for this channel will then initialize a system Master Clear followed by a system reload.

3.3.2 Single Line Communications Controller (SLCC)

The SLCC is a mono-line controller designed for high speed links operating at speeds up to 2 Mbit/s. It supports HDLC communications using the LAP.B procedure over X.21 (2 Mbit/s) or V.35 (64 kbit/s) interfaces. It is particularly suited for today's new communications techniques including high speed terrestrial lines and communication satellite links between pairs of Bull Datanets.

Figure 3-10 shows the SLCC. It comprises a mother board fitted with two daughter boards:

- data buffer,
- interface adapter.

The mother board contains the microprocessor with the following memory space:

- 8 kbytes local memory for the SLCC software,
- 1 kbyte work space containing general purpose registers, protected firmware zones and software work space,
- 16 kbytes of microprocessor firmware.

The data buffer performs:

- serial-parallel conversion,
- DMA control,
- data buffering using a FIFO register,
- CRC error checking,
- zero insertion.

The interface adapter provides the appropriate electrical interface: V.35 or X.21. It is connected to the external equipment (modem or direct connection) by a cable via the Datanet cabinet bulkhead.

When using the V.35 interface on French PTT services (TRANSPAC, TRANSFIX, TRANSCOM or TRANSDYN) a connector adapter must be fitted to the modem end of the SLCC cable.

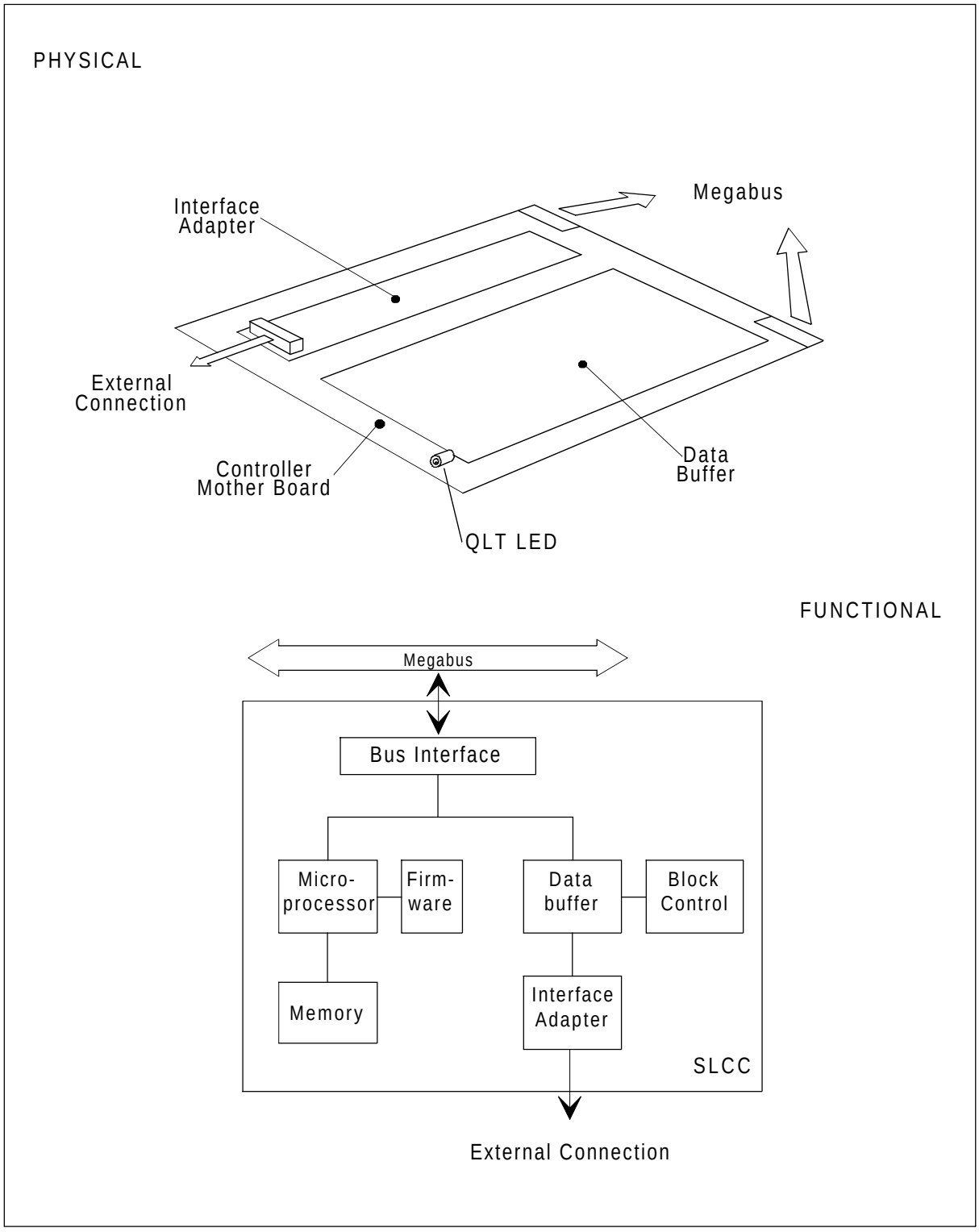


Figure 3-11. Single Line Communications Controller

3.3.3 Dual LAN Controller

The Dual LAN Controller provides two interfaces using the ISO 8802.2 and 8802.3 standard. These can be either one E-LAN (10 Mbit/s) and one StarLAN (1 Mbit/s), or two StarLAN, 1 Mbit interfaces.

The controller comprises a mother board fitted with a single daughter board (figure 3-11).

The mother board contains the microprocessor with internal memory space and the Megabus interface.

The daughter board includes a second microprocessor (the co-processor) and two serial interfaces. The serial interfaces are cabled via the bulkhead to the transceiver, which is clamped onto the LAN coaxial cable in the case of an E-LAN and to the HUB in the case of a StarLAN.

The Dual LAN Controller operates in base band mode using the CSMA/CD access procedure. Transmission speed on the E-LAN cable is 10 Mbit/s and on the StarLAN line it is 1 Mbit/s.

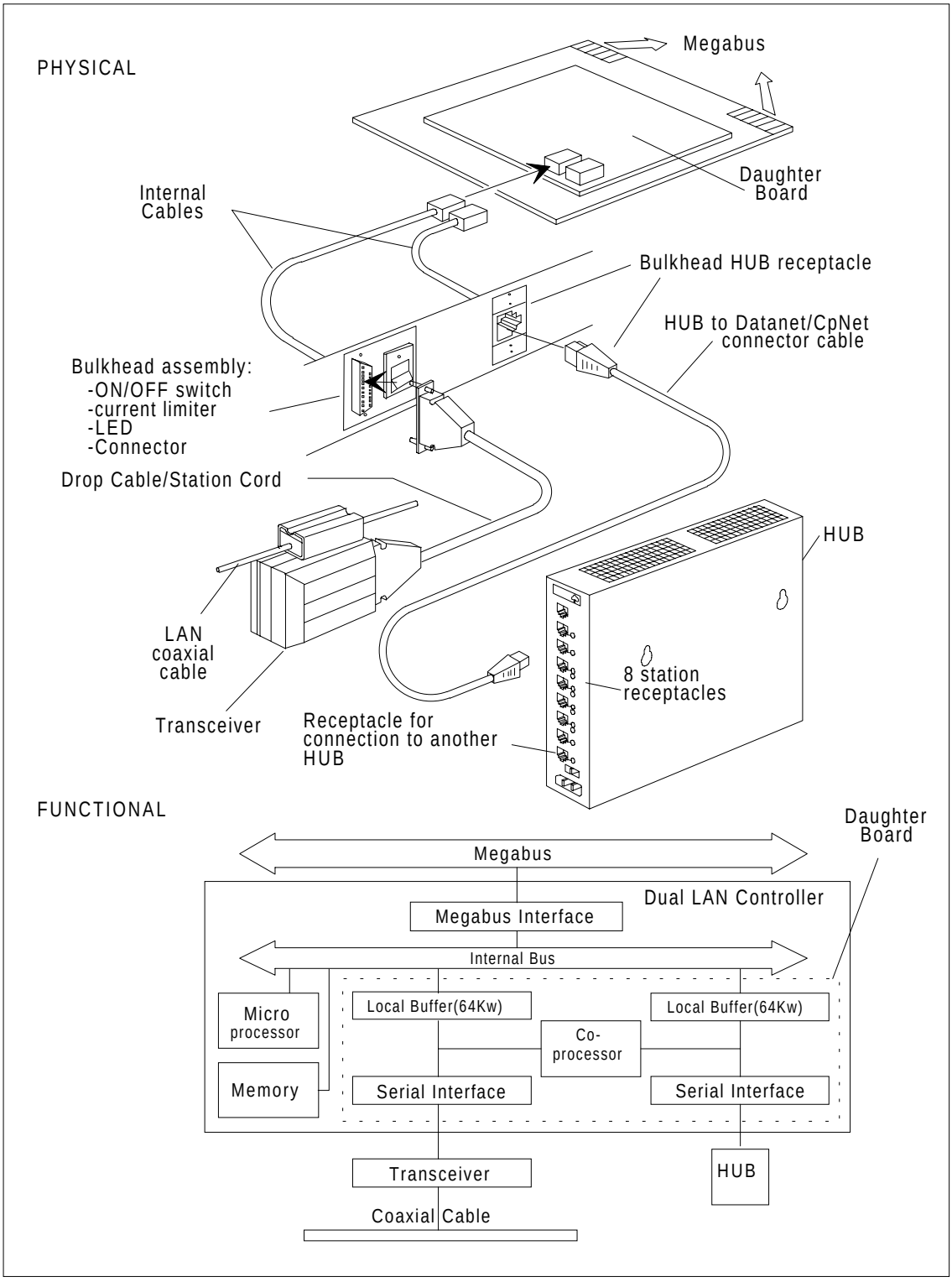


Figure 3-12. Dual LAN Controller

3.4 HOST SUBSYSTEM

The Bull Datanet host subsystem includes 3 types of host channel coupler:

- DIA (Direct Interface Attachment) to the Bull DPS 8 family of hosts,
- PSI (Peripheral System Interface) to Bull DPS 7 hosts,
- CIU (Channel Interface Unit) to IBM™ hosts.

3.4.1 Channel Interface Unit

The CIU (Channel Interface Unit) provides the interface to an IBM SNA host channel. Host processors supported include the S370 (except models 115/125), 303X, 308X, 3090, 4331, and 4341 systems. Several Bull Datanets may access the same IBM channel via the Interface Panel.

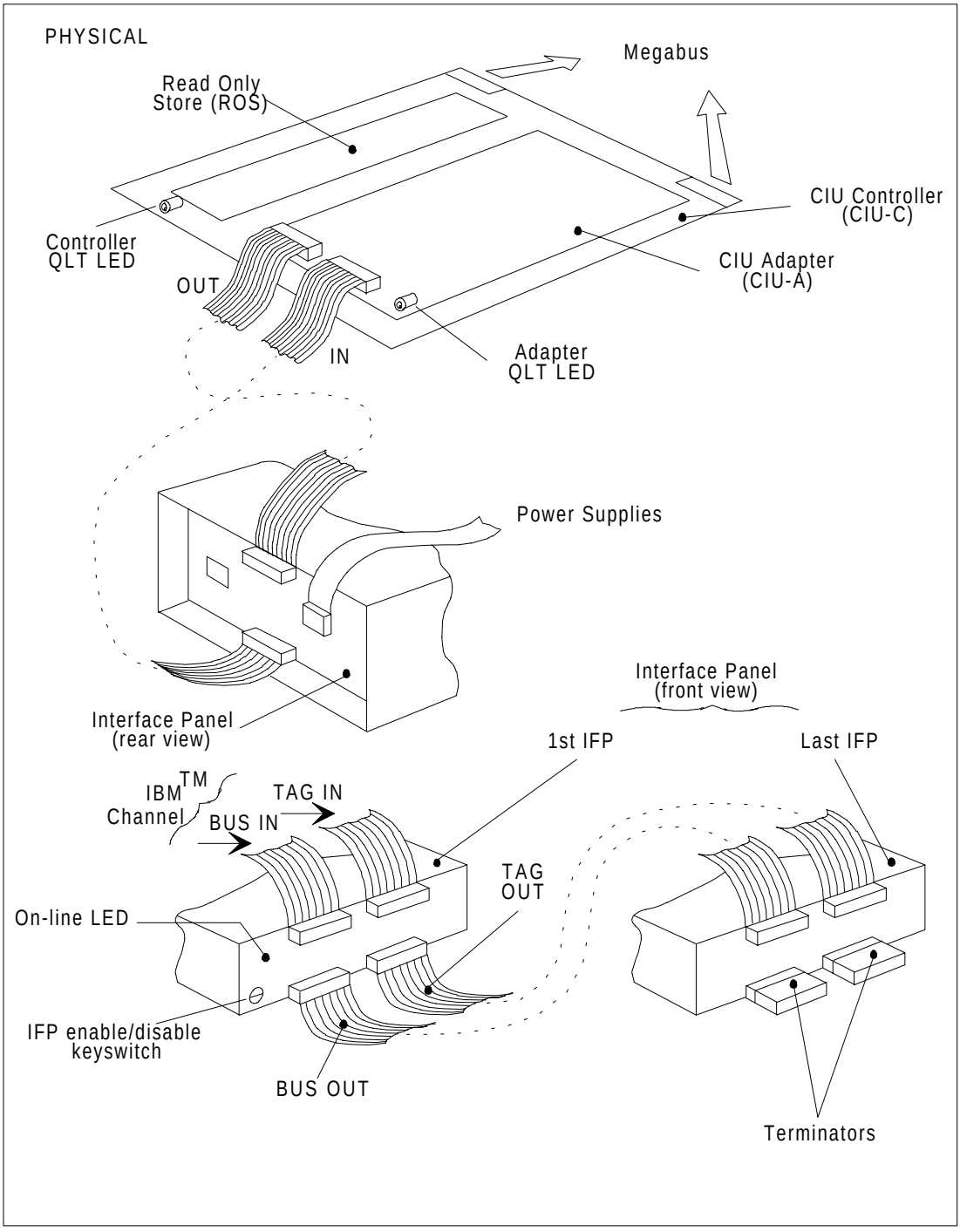
As shown in figure 3-12, a CIU subsystem comprises the following:

- a mother board, the CIU Controller (CIU-C) fitted with two daughter boards:
  - Read Only Store (ROS),
  - CIU Adapter (CIU-A),
- an Interface Panel (IFP).

The CIU-C is microprocessor based and contains the Megabus interface. It is responsible for the execution of Datanet command decoding and execution, data transfer multiplexing and status and control register storage.

The ROS contains a set of PROM chips unique to the CIU.

The CIU-A board contains the hardware necessary for dialogue with the IBM channel. Its functions include channel handshake, address and status storage, memory address counting and CIU-C interface. It is connected to the channel by two flat cables via the interface panel (IFP).



TM
This abbreviation is a trademark of the international Business Machines Corporation.

Figure 3-13. CIU Subsystem (1)

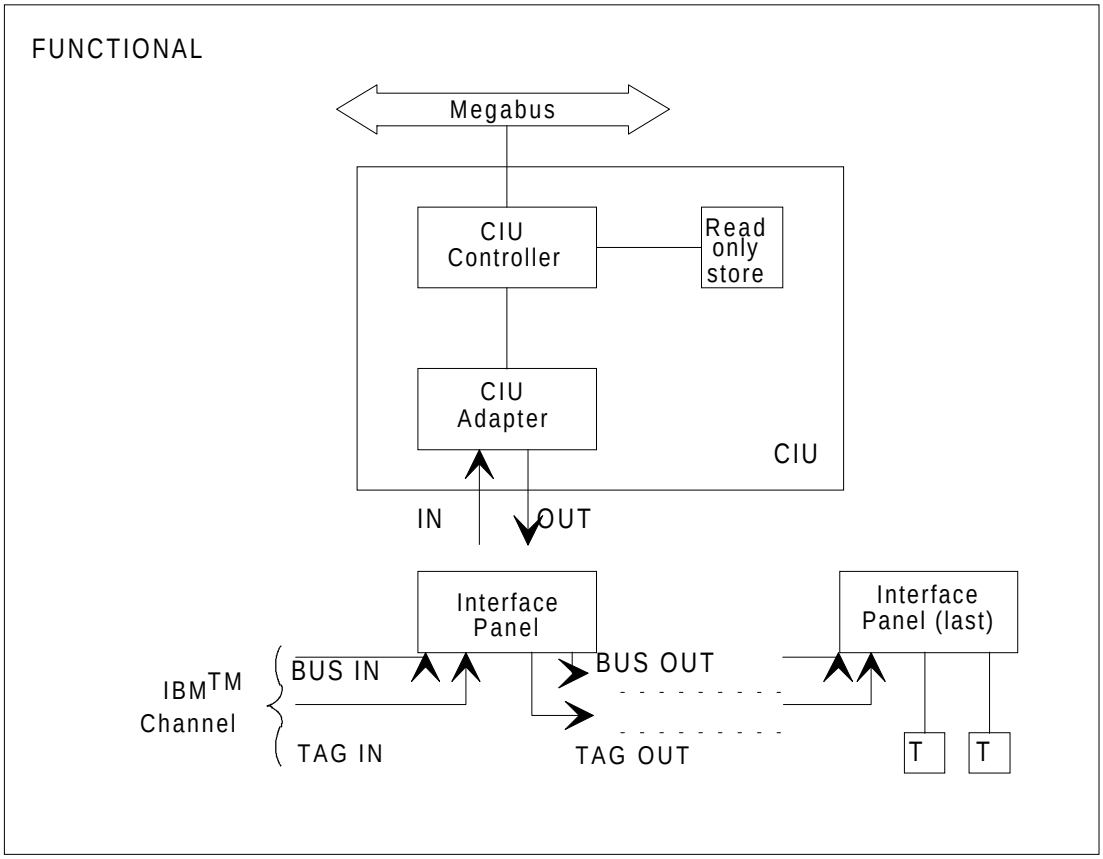


Figure 3-14. CIU Subsystem (2)

The IFP is a rack mounted panel generally located at the bottom of the Datanet cabinet. It contains the driver and receiver logic for the IBM™ channel interface lines. The panel also contains enable/disable circuits to logically and electrically disconnect the CIU from the IBM channel.

When several CIUs access the same IBM channel, they are connected in a "daisy chain" fashion. Priority logic selects one CIU at a time. The last CIU in the chain is terminated with terminator units installed on the interface panel.

3.4.2 PSI Coupler

The PSI coupler (Peripheral System Interface) provides the Bull Datanet with an interface to the PSI channel of the Bull DPS 7 family of hosts.

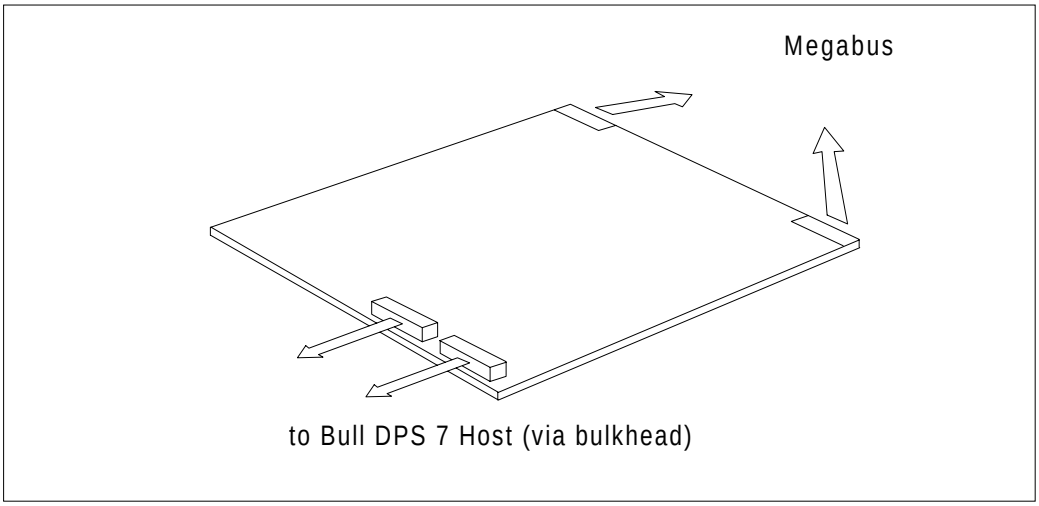


Figure 3-15. PSI Coupler

It is in the form of one mother board which contains the Megabus interface, the microprocessor with firmware store and the PSI channel interface.

The board is connected to the host by two ribbon cables via the cabinet bulkhead (figure 3-13).

3.4.3 DIA Coupler

The DIA Coupler (Direct Interface Attachment) provides the Bull Datanet with an interface to the DIA channel of the Bull DPS 8 family of hosts.

It comprises a mother board fitted with a single daughter board (figure 3-14).

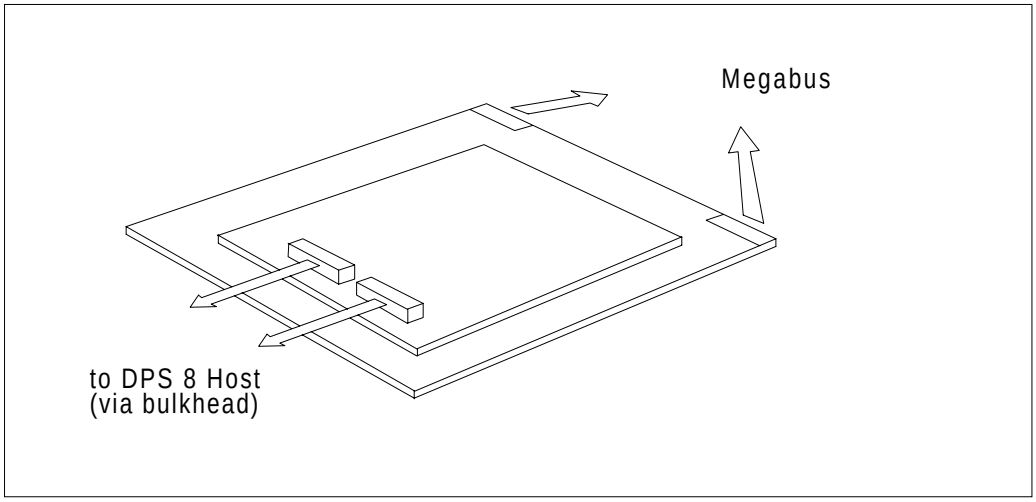


Figure 3-16. DIA Coupler

The motherboard contains the Megabus interface and microprocessor. The daughter board contains the host interface. It is connected to the host system by two ribbon cables via the bulkhead.

When a Datanet is configured with more than one DIA Coupler, it may interface with the DIA channels of several hosts or with several channels of the same host.

When operating under the GCOS 8 operating system in native mode, the host channel communicates using the CXI protocol (Common eXchange Interface). When operating under GCOS 8 in accommodation mode, the host communicates using the gateway protocol.

In both cases the hardware component is the DIA coupler.

4. Maintainability

The Datanet is provided with a complete range of tests, designed not only to be performed by the customer himself but also simple to use. Test procedures range from simple but effective microprocessor routines for hardware verification to on-line software programs capable of testing at network level.

In addition, remote access to diagnostic programs means that remote systems can be tested from a central point. Optimization of human resources can thus be obtained by centralizing competences. Tele-diagnostic, once a designer's dream is today a reality.

4.1 BULL DATANET TEST FACILITIES

Three types of test are available for checking the operation of the Bull Datanet computer system:

- Quality Logic Tests (QLT),
- Test -and Verification programs (T&V),
- In and On Line Tests (TIL).

QLTs are firmware tests implemented in the microprocessor of the individual printed circuit boards. They are automatically executed at power on and provide a rapid check of the main hardware components of each board.

T&V programs are off line software tests. They are loaded from the Datanet diskette and operate under their own operating system (TVOS). Thus the Datanet cannot be used for any networking activities during these tests. The T&V programs provide detailed checking of the internal operation of each board.

The TIL are in and on line software tests. They are executed under control of the DNS operating system. The Datanet is thus operational and can simultaneously continue its networking activities. Only the component being tested may have to be disabled during the test. The TILs perform the same checks as the T&V programs and additionally check the operation of the Datanet within the context of its network environment.

4.2 QUALITY LOGIC TESTS

The microprocessors of the CPU, memory, controllers, etc. execute routines for testing the hardware components on these boards. These are the Quality Logic Tests (QLT). The QLTs are automatically started at each system reset signal which may be generated at:

- power on,
- master clear,
- program initialization instruction.

During the execution of a QLT, a LED is lit on the edge of the board under test. At the end of the tests the LED goes out if all the checks are correct. If an error is detected, execution of the tests stops and the LED remains lit. Thus the QLTs provide a quick and easy method of pin pointing a fault to a single controller, before executing the diagnostic programs.

At power on the QLTs of the various boards of a Datanet system are executed in sequence, one after the other. The QLT LED on each board can be seen to light up as the test is executed and then go out at the end of the test (if correct) followed by the next board in the sequence.

At the same time, the word "CHECK" is continuously displayed on the 25th line of the console. The word "CHECK" disappears only when all the QLTs have been successfully executed.

In the case of the low range models, the CR41 central subsystem comprises three functions on a single board (CPU, memory, and SCF). This board comprises a single LED which may indicate a fault in any of these three areas. In order to help further localize the fault, additional information is displayed on the 25th line. This information is displayed in the form of a 4 character code following the word "CHECK".

The Dual LAN controller has 4 additional LEDs mounted on the daughter board. These are used to display an error code in the event of an unsuccessful test. This information may help to further isolate the fault by indicating whether the mother board or daughter board is the cause.

4.3 TEST AND VERIFICATION PROGRAMS

The T&V programs for the Bull Datanet are provided on two 5,25 inch diskettes. They are off line tests started up by an operator at the local console or at a remote console attached to the SCF. When the tests are started up by a remote operator, a local operator is nevertheless required to load the diskettes.

T&V programs run under control of the Test and Verification Operating System (TVOS). They check the correct operation of all circuits of the board under test. They do not however test the operation of the board in its environment. For this, the operator must use the in and on line tests.

Test results are displayed at the local and remote console. In addition, the 4 LEDs on the LAN controller daughter board are used to indicate an error code in the event of an unsuccessful test. This same information is also stored in a status word accessible to the software and to the operator(s).

It should be noted that the T&V programs are not generally available to the customer. They are intended for use by on-site maintenance technicians.

4.4 IN AND ON LINE TESTS

The in and on line tests (TIL) are specifically designed to test an operational Bull Datanet in its network environment. These tests are not limited to fault finding on Datanet systems. They are also an extremely useful tool for network optimization and tuning.

The TIL are executed under control of the OSI/DNS operating system of a Datanet. They comprise a test root resident on the Datanet and program overlays located either:

- on a diskette from which they are directly loaded onto the Datanet,
- or on the disc storage of a local or remote host processor or of a network control centre.

4.5 TELE-MAINTENANCE

Tele-maintenance or tele-diagnostic for a remote Bull Datanet can be divided into two main areas:

- use of the TIL from a remote terminal,
- use of the SCF remote console port.

Use of the TIL in a network was mentioned in the previous paragraph. Of particular interest is the flexibility of test environment provided. Thus a local or remote operator can load the tests onto a Datanet from a local host or remote system and use the tests to check the operation of this same Datanet or of another remote Datanet system.

With the SCF remote console facily (see section 3), the Datanet is open to tele-diagnostic capabilities. All control panel functions are available at the remote console. In addition the T&V and TIL are accessible to the remote operator. The remote console connection may also be used by the customer to monitor Datanet operation from a remote site.

Access security is provided by protecting the Datanet from deliberate or accidental interference from the remote terminal. The remote console procedure requires validation at the local console followed by a password entered at the remote console.

Glossary

Note: The following terms are defined as specifically used in this document.

ASF — **Administrative Storage Facility**
That part of DSAC which provides a logging capability by which distributed system statistics can be collected and by which system history can be examined and validated by other administrative functions. The Administrative Storage Facility may be distributed as appropriate. The NAD at a system with no ASF will utilize an ASF at some other system(s).

AUT — **Administrative UTility**
Administrative Utilities are a set of batch or real-time utility programs used in support of DSAC functions. Several types of AUTs are possible. User-written AUTs (JAUT) can customize network administration for specific applications.

BOOT — **Bootstrap Routine**
A firmware routine used to read the computer software into the main memory.

BPF — **Boot PROM FLAP**
A FLAP fitted with a PROM which contains the bootstrap routine.

BSC — **Binary Synchronous Communications**
An IBM[TM] line protocol used by certain synchronous terminals.

CCP — **Channel Control Program**
A software module responsible for the management of one communications channel.

CIU — **Channel Interface Unit**
Hardware unit used to interface the Bull Datanet to an IBM host processor channel.

[TM] This abbreviation is a trademark of the International Business Machines Corporation.

CPU — **Central Processor Unit**
The central hardware unit of the computer. It executes the instructions of the software.

<CR> — **Carriage Return**
The carriage return key of a typewriter keyboard. On electronic terminals this key may be engraved: enter, ENT, transmit, etc.

CRC — **Cyclic Redundancy Check**
A method of checking for errors in transmitted and received data.

CSMA/CD — **Carrier Sense Multiple Access with Collision Detection**
An ECMA link layer protocol for communications via a LAN.

CSS — **Central Subsystem**
Central hardware of the Bull Datanet comprising the CPU, memory, and SCF.

DCE — **Data Circuit-terminating Equipment**
This equipment (modems (data-sets), auto-dialers, limited distance modems and modem eliminators) is used to adapt the signals sent by DTE (Data Terminal Equipment) to the line to be used, and convert signals received to a form appropriate to the DTE.

DIA — **Direct Interface Attachment**
A communications channel of the Bull DPS 8 family of host processors.

Also used as an abbreviation for the DIA Coupler which is a hardware unit used to interface the Bull Datanet to the DIA channel of a Bull DPS 8 host.

DMA — **Direct Memory Access**
A procedure by which controllers access main memory directly. The transfer of data to or from memory is initialized by the CPU but the actual transfer process is executed by the controller without CPU intervention. In this way I/O operations can occur simultaneously with CPU internal processing.

DNS — **Distributed Network Supervisor**
The operating system of the Bull Datanet and CpNet.

DPS — **Distributed Processing System**
Bull's range of computer hardware designed principally for operating in distributed environments. The range includes the Bull DPS 6 satellite and the Bull DPS 7 and 8 host processors.

DSA — **Distributed Systems Architecture**
Bull's standard for the design of distributed systems. It is a specification of the system functions needed to support distributed application programs and the protocols and interfaces by which these system functions coordinate their activities. DSA is the standard set of rules for developing distributed systems products. It conforms to the ISO model for Open Systems Interconnection.

DSAC — **Distributed Systems Administration and Control**
The set of functions required for coordinated management of every part of a distributed system including status monitoring, statistics collection, failure recovery, maintenance, systems generation and modification. Network Operator Interfaces, via which an operator can access the DSAC functions, may be centralized at a Network Management Facility (NMF) or distributed.

DTE — **Data Terminal Equipment**
Terminal or host system equipment intended to be connected to another DTE by either point-to-point or multipoint line configuration for data transfer, via DCE (Data Circuit terminating Equipment), where this latter is necessary

Dual LAN Controller — **Dual Local Area Network Controller**
A LAN controller that provides connection to two Local Area Networks. These can be either both in the StarLAN configuration, or one StarLAN (1 Mbits/s) and the other of the E-LAN (10 Mbits/s).

EDAC — **Error Detection And Correction**
A system of logic used in the memory modules of the Bull Datanet. This system detects and corrects single bit errors.

E-LAN — **Bull Establishement-Local Area Network**
An Ethernet[TM1] type Local Area Network which uses a coaxial cable to connect different network stations via transceivers.

FCP — **Full Control Panel**
A maintenance panel fitted to earlier versions of the Bull Datanet. It was used for starting and loading the system, displaying CPU status information and for communicating directly with the CPU and the operating system.

FEP — **Front End Processor**
A network processor which provides communications management services and terminal management facilities for an information processor to which it is directly attached.
The Bull Datanet can function as a FEP, the CpNet can not.

[TM1] This abbreviation is a trademark of the Digital Equipment Company.

FIFO — **First-In First-Out Register**
A buffer where data is read out, in the same order as it was written in.

FLAP — **Flexible Line Adaptor Package**
A hardware unit connected via a cable to an LA of the MLX-16 communications controller. It is generally used to provide the electrical interface between the LA and the modem or communications line. One exception to this rule is the BPF.

GCOS — **General Comprehensive Operating System**
The operating system for Bull's DPS range of processors. The Bull DPS 6 runs on GCOS 6, the Bull DPS 7 runs on GCOS 7 and the Bull DPS 8 runs on GCOS 8.

HDLC — **High Level Data Link Control**

ISO/CCITT — **standard link protocol used in DSA.**

I/O — **Input and Output**

IFP — **InterFace Panel**

A hardware unit used for interfacing several CIUs to a single IBM[TM] host channel. Each CIU is attached to its own IFP and the IFPs are connected in daisy chain to the host channel.

ISO — **International Standards Organization**
This abbreviation is still sometimes used to designate the ISO architecture for Open Systems Interconnection (OSI) reference model.

LA — **Line Adapter**
A hardware unit plugged into the MLX-16 communications controller. The LA provides support of the specific line procedure used by the communications link connected either directly to the LA or via a FLAP.

LAF — **Long Address Format**
A logical memory addressing format used on all DN 71XX models which permits addressing up to 2 Mbytes.

LAN — **Local Area Network**
A type of communications system which provides links within a restricted distance (a building or building complex) at speeds up to 10 Mbits/s.

[TM] This abbreviation is a trademark of the International Business Machines Corporation.

LAP — **Link Access Procedure**
A procedure which defines data exchange between the DTE and DCE at the link level. The procedures used in DSA are the HDLC LAP.B (for point-to-point links) and HDLC NRM (for multi-point). HDLC NRM is also referred to as LAP.N in DNS documentation.

LED — **Light Emitting Diode**
Used as a luminous indicator of the operation of hardware components.

LIU — **Line Interface Unit**
Synonym for FLAP.

MDC — **Multi-Device Controller**
A hardware component used to control the diskette drive. The MDC type III used on the DN 713X is also fitted with the console adapter which is the component via which the software communicates with the system control facility.

MLX-16 — **Multi-Line, Multi-System Controller**
A hardware component used to control up to 16 communications lines. The MLX-16 is adapted to the type(s) of line being used by fitting line adaptors to it.

MMPO — **Main Memory PROM Option**
A hardware component fitted to earlier models of the Bull Datanet. It performed the functions of the BPF.

MMU — **Memory Management Unit**
Memory control logic.

NAD — **Node ADministrator**
The component of DSAC which is required in each system and is responsible for making the required control actions happen in the system, as well as reporting local events of interest to the outside world.

NIM — **Network Interface Module**
A Bull terminal concentrator enabling connection of asynchronous terminals directly to E-LAN or StarLAN Local Area Networks.

NOI — **Network Operator Interface**
A component of DSAC which supports operator or administrator connection to a set of NADs (or AUTs) in a network. It translates the Administrative Control Language (used by the operator) to/from Administrative Exchange Protocol (used by the NAD and ASF.

NRM — **Normal Response Mode**
Link level protocol used in HDLC multi-point communications. It is also referred to as LAP.N in DNS documentation.

OSF — **Open Systems Facilities**
Products and facilities offered by Bull for the interconnection of DSA with other network architectures.

OSI — **Open Systems Interconnection**
An ISO term, also called the OSI Reference Model. The word "open" refers to the ability to connect together into cooperating relationships any systems which conform to the OSI Architecture.

PABX — **Private Automatic Branch eXchange**
An electronic switch used for selecting telephone lines at a private telephone switch board.

PAD — **Packet Assembler Disassembler**
The transformations required to provide connections between TTY terminals and a host system via an X.25 Network are supplied by a PAD. The terminal-to-PAD link operates under X.28, and is typically supplied by the VAN supplier. The PAD-to-Terminal Management link operates under the X.29 protocol over the X.25 network.

PDN — **Public Data Network**
Any communications network available for use by the public. Normally this refers to the telephone network, or a network controlled by the national telecommunications administration or any other common carrier.

PSI — **Peripheral System Interface**
A communications channel of the Bull DPS 7 host processors.

Also used as an abbreviation for the PSI Coupler which is a hardware unit used to interface the Bull Datanet to the PSI channel of a Bull DPS 7 host.

PTT — **Postes et Télécommunications**
The French public telecommunications administration.

QLT — **Quality Logic Tests**
Firmware routines resident on printed circuit boards used for testing the board hardware.

RCI — **Remote Computer Interface**
A pre-DSA protocol used for communicating with small, remote, computer systems.

ROS — **Read-Only Store**
A daughter board fitted to the CIU containing ROM.

SCA — **System Control Adapter board**
A hardware unit containing the system control facility logic on the DN 7100/XX models.

SCF — **System Control Facility**
A combination of hardware and firmware which provides the operator's interface to the Bull Datanet, models DN 713X.

SCP — **System Control Panel**
The computer control panel fitted to DN 71XX models.

SLCC — **Single Line Communications Controller**
A hardware communications controller used to control one high speed communications line.

SNA[TM] — **Systems Network Architecture**
IBM's standard for the design of distributed systems.

StarLAN — **Star type Local Area Network**
A Local Area Network using twisted pair wiring and Bull HUBs to create local networks with star type configurations. A StarLAN operates at a speed of 1 Mbits/s.

T&V — **Test and Verification programs**
Software tests for the Bull Datanet, used by maintenance technicians. The T&V programs run under control of TVOS, thus when running these tests, the Datanet is off-line.

TIL — **In and On Line Tests**
Software tests for the Bull Datanet, used by the customer. The TIL run under control of DNS, thus when running these tests, the Datanet remains on-line.

TTY — **Tele-TYpe**
A line procedure used by tele-type terminals.

TVOS — **Test and Verification Operating System**
The operating system (or monitor) for the T&V programs.

VAN — **Value Added Network**
A communications network in which network services (e.g., Transport Services, Packet Switching, etc.) are leased from a third party as a value-added service; some examples include: Transpac, Datapac, Telenet, Tymnet, Euronet and Nordic Public Data network. Often called a public data network.

VCP — **Virtual Control Panel facility**
The logic which controls the control panel functions of the Bull Datanet. These functions include display of status information at the console screen and execution of control panel commands (LOAD, RUN, EXECUTE etc.) entered at the console keyboard. On earlier models of the Datanet they were performed by a real control panel, the FCP. Hence the term "Virtual" control panel.

[TM] This abbreviation is a trademark of the International Business Machines Corporation

VIDEOPAD **Video PAD**
An extension of the PAD facility which provides an access to X.25 networks for Videotex type terminals (e.g. Minitel in France).

VIP **Visual Interface Presentation**
A screen presentation protocol used by certain synchronous and asynchronous terminals.
There also exists a VIP line procedure which is a synchronous procedure (and therefore not used by asynchronous terminals).

WAN **Wide Area Network**
A communications network providing data communications over large distances. WANs include private and public X.25 networks and public X.21 networks. Also, all VANs are WANs.

Index

H

I

L

M

N

O

P

Q

R

S

T

V

W

X

Y

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