

Real-Time Neutron and Alpha Soft-Error Rate Testing of CMOS 130nm SRAM: Altitude *versus* Underground Measurements

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Abstract— This work reports real-time soft-error rate (SER) testing of semiconductor static memories in both altitude and underground environments to separate the component of the SER induced by the cosmic rays (i.e. primarily by atmospheric neutrons) from that caused by on-chip radioactive impurities (alpha-particle emitters). Two European dedicated sites were used to perform long-term real-time measurements with the same setup: the Altitude SEE Test European Platform (ASTEP) at the altitude of 2252m and the underground laboratory of Modane (LSM, CEA-CNRS) under 1700 m of rock (4800 meters water equivalent). Experimental data obtained using 3.6 Gbit of SRAMs manufactured in CMOS 130 nm technology are reported and analyzed. Comparison with accelerated and simulated SER is also discussed.

Index Terms— Single-Event Rate (SER), real-time testing, atmospheric neutrons, terrestrial radiation environment, static memory, accelerated tests, SER simulation, alpha contamination, neutron-induced SER.

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I. INTRODUCTION

AS Metal-Oxide-Semiconductor (MOS) devices continue to be scaled down, the sensitivity of integrated circuits to radiation coming from the natural terrestrial environment (primarily atmospheric neutrons) or induced by on-chip radioactive impurities (source of alpha particles) has been found to seriously increase and at least sufficiently to be considered as a major reliability problem by several semiconductor manufacturers [1]. Current ultra-scaled memory ICs become more and more sensitive to single-event-upset (SEU) because of the constant reduction of the supply voltage and node capacitance, resulting in a decrease of the so-called “critical charge” used to store logical information [2-3]. However, the sensitivity of a given technology to atmospheric neutrons or alpha emitters (present into the chip) has not necessary the same magnitude and its impact on the soft-error rate (SER) must be carefully evaluated, i.e. separated in terms of fail occurrence or failure-in-time (FIT).

This work precisely deals with the experimental determination of neutron and alpha induced SER from long-term real-time experiments performed in two very different environments: the first one in altitude to strengthen natural neutron irradiation, the second one underground to completely screen this atmospheric contribution and to quantify the remaining alpha SER directly induced by the presence of radioactive impurities of alpha emitters (Pb, U, Th,...) in the chip materials. Tests have been performed using a CMOS 130nm commercial technology; no BPSG was used in the Back-End Of Line (BEOL) of our DUTs, thus eliminating the major source of ¹⁰B in the circuits and drastically reducing their possible interaction with low energy neutrons (in the thermal range and below) [1-3].

The paper briefly describes, in section II, the test environments, equipment and circuits used in this study before detailing and analyzing real-time experimental data in section III. Comparison with accelerated SER is finally presented to accurately evaluate the alpha emissivity of circuit materials.

II. TEST PLATFORMS AND EXPERIMENTAL DETAILS

Real-time SER tests were successively performed on two dedicated sites with exactly the same setup, including the automatic test equipment, the control software and more than one thousand SRAM memory ICs. Altitude measurements

TABLE I
LOCATION AND MAIN ENVIRONMENT CHARACTERISTICS OF THE ASTEP
PLATFORM (AFTER REF. [5]).

ASTEP, Plateau de Bure, France		
Latitude (°N)	44.6	
Longitude (°E)	5.9	
Elevation (m)	2552	
Atm. depth (g/cm ²)	757	
Cutoff rigidity (GV)	5.0	
Relative neutron flux	Active Sun low	5.76
	Quiet Sun peak	6.66
	Average	6.21

were performed during the period March 31, 2006 – November 26, 2006 on the ASTEP platform at the altitude of 2252m with respect to sea level. Since October 16, 2007, the experiment has been running at the underground laboratory of Modane (LSM) in a low cosmic ray environment to detect and quantify the part of the SER induced by internal (i.e. on-chip) radioactive contamination. In the following, we briefly describe the test environments and give some key details about the test equipment, the SRAMs and the test procedure used.

A. The ASTEP platform

ASTEP is a dual academic research and R&D platform founded by STMicroelectronics, JB R&D and L2MP-CNRS in 2004 [4]. The current platform, operated by IM2NP-CNRS (formerly L2MP), is dedicated to real-time SER testing of semiconductor circuits and systems. Located in the French Alps on the desert Plateau de Bure at 2552m, in a low electromagnetic noise environment, the platform is hosted by the Institute for Radio-astronomy at Millimeter Wavelengths (IRAM). The ASTEP platform is installed in an ancient radio-telescope building reconverted into an altitude laboratory platform (one floor standard concrete slab building). ASTEP is fully operational since March 2006 and is referenced in the JEDEC standard JESD89A [5]. In complement to SER testing facilities, ASTEP is now providing in situ real-time neutron monitoring using a super 3-NM64 neutron monitor. Table I gives the main environment characteristics of the ASTEP platform, as reported in Table A3.B of Ref. [5].

B. The underground laboratory of Modane (LSM)

The underground laboratory of Modane is located about 1700 m under the top of the Fréjus mountain (4800 meters water equivalent), near the middle of the Fréjus highway tunnel connecting France and Italy [6]. It was created in 1983 in order to conduct particle physics and astrophysics experiments in a strongly reduced cosmic ray background environment. Due to the depth of the LSM, the particle flux inside the laboratory is extremely reduced:

- 4 muons/m²/day corresponding to a two million reduction factor compared to the flux at sea level;
- 3x10³ fast neutrons/m²/day (in the energy range 2-6 MeV) emitted by natural radioactivity from the rock, the neutron component of cosmic rays being totally eliminated at this depth. Table II gives measured radioactivity levels of the rock and concrete obtained by gamma spectrometry.

TABLE II
RADIOACTIVITY LEVELS OF THE LSM CAVITY ROCK AND CONCRETE [6].

	²³⁸ U	²³² Th	⁴⁰ K
Rock	(0.84±0.2) ppm	(2.45±0.2) ppm	(0.213±0.03) Bq.g ⁻¹
Concrete	(1.9±0.2) ppm	(1.4±0.2) ppm	(7.73±1.3)×10 ⁻² Bq.g ⁻¹

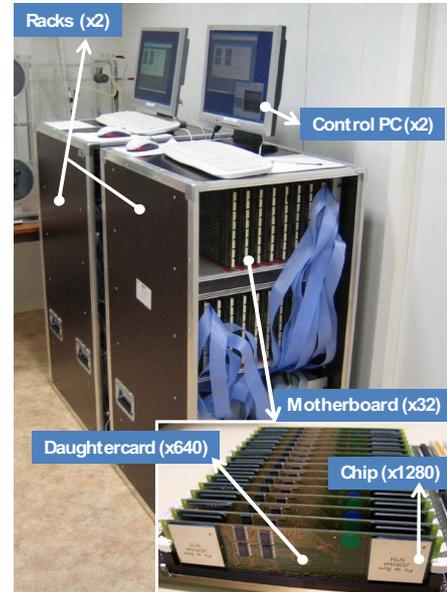


Fig. 1. General view of the SRAM automatic test equipment (here photographed at LSM). Inset: detail of one motherboard containing 40 daughtercards and 80 test chips (2 per daughtercard). The complete system is designed to test a maximum of 1280 chips dispatched on 32 motherboards and 640 daughtercards.

Finally, the Radon in the laboratory is maintained at a very low rate of ~20 Bq/m³ owing to a air purification system which totally renews the volume of the air inside the laboratory twice an hour.

C. Test equipment, circuits and procedure

Fig. 1 shows the SRAM automatic test equipment, specially designed and constructed for the study. This system is capable of monitoring several thousands of synchronous/asynchronous SRAM memories and performing all requested operations such as writing/reading data to the chips, comparing the output data to the written data and recording details on the different detected errors. The complete system has been described in detail in Refs. [4,7]. The different hardware and software components have been designed to strictly follow all the specifications of the JEDEC Standard JESD89A [5]. Particular precautions were taken to minimize digital noise sources and to discriminate memory soft errors from eventual transient errors possibly induced by the system itself. For maximizing the test equipment stability, the control PC and the DUTs should have been ideally split into two different locations. However, Refs. [2,8] with similar system configurations as ours have not reported any test artifact due to its compactness.

Real-time measurements have been currently performed on bulk SRAMs fabricated by STMicroelectronics using a CMOS 130nm commercial technology process, PBSP-free as previously mentioned. This technology was extensively

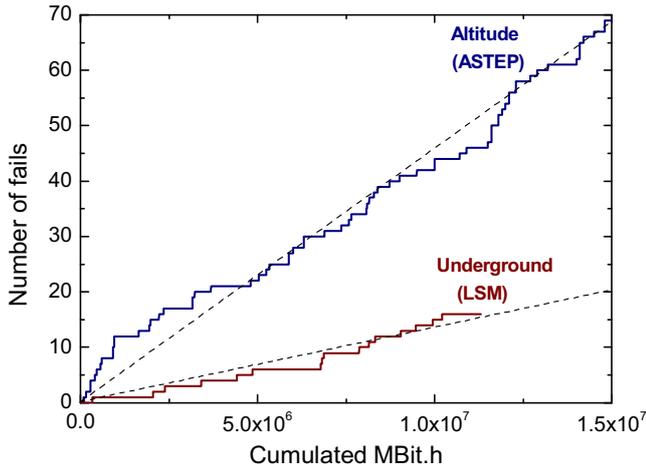


Fig. 2. Cumulative fail numbers versus cumulated number of MBit×h for the two experiments conducted in altitude and underground. The experiment periods are [March 31, 2006 – November 6, 2006] for the altitude test and [October 16, 2007 – February 27, 2008] for the underground test. For both experiments, tests have been conducted under nominal conditions: $V_{DD}=1.2V$, room temperature, standard checkerboard test pattern. A cumulated number of MBit×h > 10⁷ MBit×h gives an excellent confidence interval on the extrapolated SER for both experiments.

characterized in previous works using alpha irradiations and neutron accelerated SER tests performed with two continuous neutron sources available in North-America (TRIUMF and LANSCE facilities). The SRAM elementary memory point corresponds to a 6-transistor cell with a bit cell area of 2.50 μm^2 . The test chip capacity is 4 MBit ; 912 chips, i.e. 3,664 MBit, have been considered for performing the experiment.

III. RESULTS AND DISCUSSION

In the following, all numerical results have been normalized by a common arbitrary scaling factor, set lower than 3×. The real order of magnitude for the reported data is thus not significantly altered. Fig. 2 shows the cumulative fail number versus cumulated number of MBit×h for the two experiments. A total of 69 fails was detected after 1.50×10^7 MBit×h in altitude, 16 fails after 1.05×10^7 MBit×h during the underground test. Experimental data consistency (i.e. compliant with a “random process”) was checked for both experiments in terms of statistical distribution of 0→1 and 1→0 bit flips and error bitmap: the frequency of bit flips is found very close to 50% for each transition which are randomly distributed in the memory plan. From data of Fig. 2, we estimated the real-time SER at the test location, shown in Figs. 3 and 4, using the following expression:

$$SER = \frac{N_r}{\Sigma_r} \times 10^9 \text{ (FIT/MBit)} \quad (1)$$

where N_r is the number of fails observed at time T_r and Σ_r is the number of MBit×h cumulated at time T_r .

Figs. 3 and 4 show that the convergence of SER vs. test hours is asymptotically reached within ~3000 h. Beyond this duration, the SER remains constant around 4658 FIT/MBit for the altitude experiment and around 1530 FIT/MBit for the underground test.

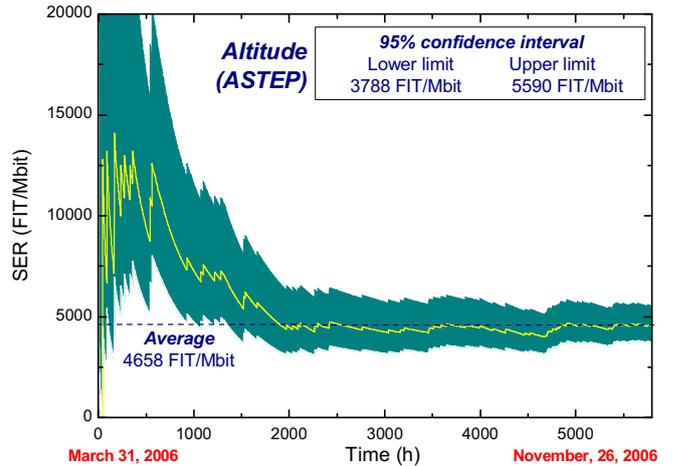


Fig. 3. Real-time SER (FIT/MBit) versus test hours calculated from data of Fig. 2 for the altitude experiment. 95% confidence intervals are also indicated. The SER rate indicated here is given at ASTEP altitude, i.e. not normalized to sea level. The erratic character and high value of the SER in the first ~1000 hours are due to the very low number of cumulated fails during this initial period, introducing a large error in the evaluation of the ratio N_r/Σ_r in Eq. (1).

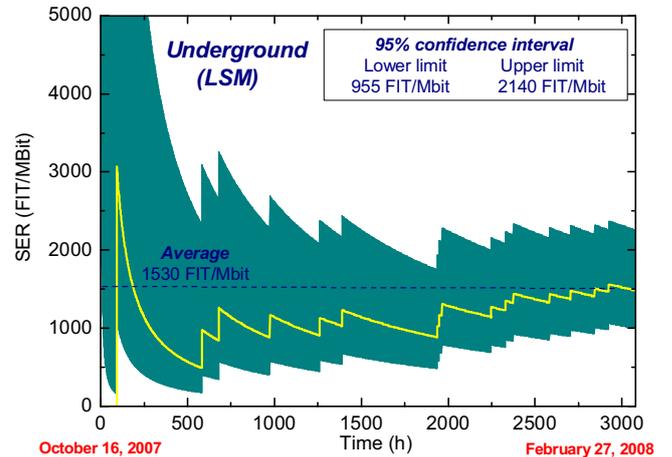


Fig. 4. Same legend as in Fig. 3 with a SER rate corresponding this time to data of Fig. 2 for the underground experiment.

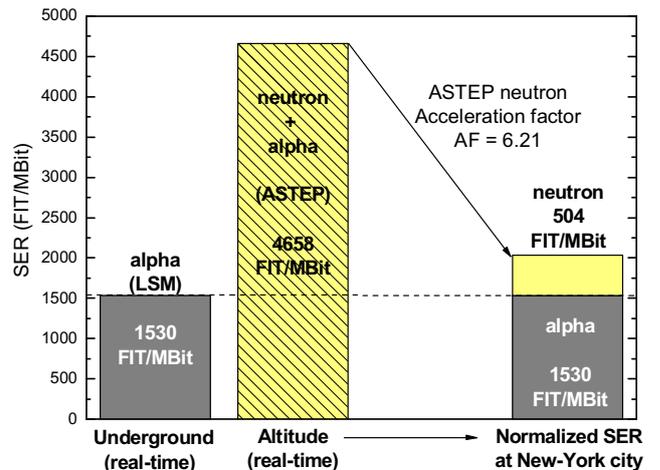


Fig. 5. Synthesis of experimental real-time SER values obtained from altitude and underground experiments and normalization of the SER at the reference flux of New-York City (sea-level) [5] taking into account i) the alpha contribution for the altitude test (fixed to the value measured at LSM) and ii) the ASTEP acceleration factor $AF=6.21$ for the neutron flux in altitude.

TABLE III
SUMMARY OF SER VALUES (FIT/MBIT) OBTAINED FROM ACCELERATED AND REAL-TIME DATA

	α -SER	n-SER
SER from accelerated test at sea-level [4]	380 (1)	665
SER from real-time at ASTEP location	1530 (2)	4658
SER from real-time at sea-level	1530 (2)	504

(1) Assuming an alpha-emissivity of 10^{-3} alpha/cm²/h for the semiconductor processing and packaging materials

(2) Assuming an alpha-emissivity of 4×10^{-3} alpha/cm²/h.

The calculation of the normalized real-time SER at the reference location of New-York City (i.e. sea-level) is illustrated in Fig. 5. Assuming an acceleration factor AF=6.21 for the ASTEP location and a fail rate due to alphas identical to the alpha-SER experimentally deduced from underground experiment, the normalized neutron-SER is then given by:

$$neutron-SER|_{NYC} = \frac{SER|_{ASTEP} - SER|_{LSM}}{AF} = 504 \text{ FIT/MBit (2)}$$

which leads to a total SER = 2034 FIT/MBit for both alpha and neutron contributions.

Table III recapitulates the different alpha and neutron SER values obtained from accelerated (previous work, see Ref. [4]) and real-time (this work) data. In Ref. [4], the alpha-SER was evaluated from accelerated measurements using an intense Am²⁴¹ alpha source. At that time of study and in lack of both underground and alpha-emission characterizations, this value was obtained assuming for the semiconductor processing and packaging materials a natural alpha emissivity of 10^{-3} alpha/cm²/h. This default value, that corresponds to an "ultra low alpha" grade [2], led to an alpha-SER=380 FIT/MBit. In the present work, the alpha emission rates for both the tested wafers and packages (mold compound) were accurately characterized using an ultra-low alpha background counter (gas flow type). A very high purity in terms of radioactive contaminants was confirmed, around 2×10^{-3} alpha/cm²/h. Now, if we consider accelerated and real-time alpha SER, the best agreement between these two values is found for an alpha emission rate equal to 4×10^{-3} alpha/cm²/h. This discrepancy between 10^{-3} and 4×10^{-3} is small and acceptable with respect to the experimental uncertainties for the alpha counting, the SER testing and the lot-to-lot variations for the trace amounts of alpha contaminants. As a result, the total (alpha+neutron) accelerated SER is then equal to 1530 + 665 = 2195 FIT/MBit. This value is within the experimental error margins with respect to the total real-time SER value of 2034 FIT/MBit. Contrary to that reported in [9], we thus found that accelerated and real-time experiments give very close results for neutrons, respectively 665 and 504 FIT/MBit. These values are also very consistent with 3D SER simulation results (ST-proprietary simulation code [10-11]) that give a neutron-SER value around 700 FIT/MBit.

IV. CONCLUSION

We reported in this work real-time soft-error rate testing of 3.6 Gbit of bulk SRAMs manufactured in CMOS 130 nm technology in both altitude and underground environments. The combination of these two tests allowed us to separate the

component of the SER induced by atmospheric neutrons from that caused by on-chip alpha-particle emitters. In the particular case of the present tested SRAMs, this later is found to be three times larger than the neutron contribution at sea-level. This study also highlights the importance of combining real-time, accelerated and alpha-emission characterization, to accurately estimate the soft-error rate of a given technology. Such a multi-characterization approach should ensure that the different extracted values are consistent with the underlying calculation hypothesis and are within experimental error margins.

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REFERENCES

- [1] P. Roche, "Year-in-Review on radiation-induced Soft Error Rate", tutorial at IEEE International Reliability Physics Symposium, San Jose, USA, March 2006.
- [2] J.F. Ziegler, H. Puchner, SER – History, Trends and Challenges, Cypress Semiconductor, 2004. See also references therein.
- [3] R.C. Baumann, "Radiation-Induced Soft Errors in Advanced Semiconductor Technologies", IEEE Transactions on Device and Material Reliability, Volume 5, N°3, pp. 305-316, 2005.
- [4] J.L. Autran, P. Roche, J. Borel, C. Sudre, K. Castellani-Coulié, D. Munteanu, T. Parrassin, G. Gasiot, J.P. Schoellkopf, "Altitude SEE Test European Platform (ASTEP) and First Results in CMOS 130nm SRAM", IEEE Transactions on Nuclear Science, 2007, Vol. 54, n°4, p. 1002-1009.
- [5] JEDEC Standard Measurement and Reporting of Alpha Particles and Terrestrial Cosmic Ray-Induced Soft Errors in Semiconductor Devices, JESD89 Arlington, VA: JEDEC Solid State Technology Association Available online: <http://www.jedec.org/download/search/JESD89A.pdf>.
- [6] V. Chazal, R. Brissot, J.F. Cavaignac, B. Chambon, M. De Jésus, D. Drain, Y. Giraud-Héraud, C. Pastor, A. Stutz, L. Vagneron, "Neutron background measurements in the underground laboratory of Modane", Astroparticle Physics, 1998, Vol. 9 p. 163-172.
- [7] J.L. Autran, P. Roche, G. Gasiot, T. Parrassin, J.P. Schoellkopf, J. Borel, "Real-time Soft-Error Rate Testing of Semiconductor Memories on the European Test Platform ASTEP", Proceedings of the 2nd International Conference on Memory Technology and Design (ICMTD 2007), Giens, France, 7-10 mai 2007, p. 161-164.
- [8] T. J. O'Gorman, J. M. Ross, A. H. Taber, J. F. Ziegler, H. P. Muhlfield, C. J. Montrose, H. W. Curtis, J. L. Walsh, "Field testing for cosmic ray soft errors in semiconductor memories", IBM J. Res. Dev., 1996, Vol. 40, N°1, p. 41-50.
- [9] H. Kobayashi, H. Usuki, K. Shiraishi, H. Tsuchiya, N. Kawamoto, G. Merchant, J. Kase, "Comparison Between Neutron-Induced System-SER And Accelerated-SER in SRAMs", Proceedings of the IEEE International Reliability Physics Symposium, Phoenix, USA, pp. 288-293, 2004.
- [10] P. Roche, G. Gasiot, "Impacts of Front-End and Middle-End Process Modifications on Terrestrial Soft Error Rate", IEEE Transactions on Device and Materials Reliability, Volume 5, N°3, pp. 382-396, 2005.
- [11] P. Roche, G. Gasiot et al., "Comparisons of Soft Error Rate for SRAMs in Commercial SOI and Bulk below the 130 nm Technology Node", IEEE Transactions on Nuclear Science, Volume 50, N°6, pp. 2046-2054, 2003.